Description

CambridgeIC's CAM312 Central Tracking Unit (CTU) chip is a single-chip processor for position measurement. It implements the electronic processing for resonant inductive position sensing technology.

The CAM312 measures the position of contactless, inductively coupled targets relative to sensors that are built from printed circuit boards to CambridgeIC's designs.

The CAM312 supports a wide variety of different sensors, including rotary, linear and arc.

Features

- Resonant inductive position sensing engine
- Fully ratiometric measurements
- Automatic tuning to target frequency
- Fast SPI communications (slave device)
- User IOs for sample indicators
- Measures two Type 4 sensors or one Type 2 or 6
- SPI interface checksum available for integrity check
- Internal software upgradable over SPI

Performance

- Up to 2000 position samples per second
- Resonator frequency tuning range at least ±10%
- Short Group Delay of 200µs
- Noise Free Resolution 10…15 bits depending on sensor

Product identification	
Part no.	**Description**
CAM312ME	28-pin QFN -40°C to 125°C
CAM312MA	28-pin QFN -40°C to 150°C

Figure 1 CAM312ME image

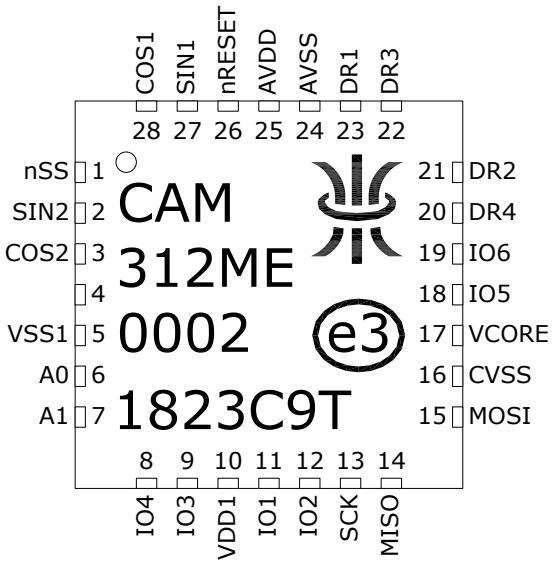

Figure 2 CAM204BE 28-pin SSOP pinout

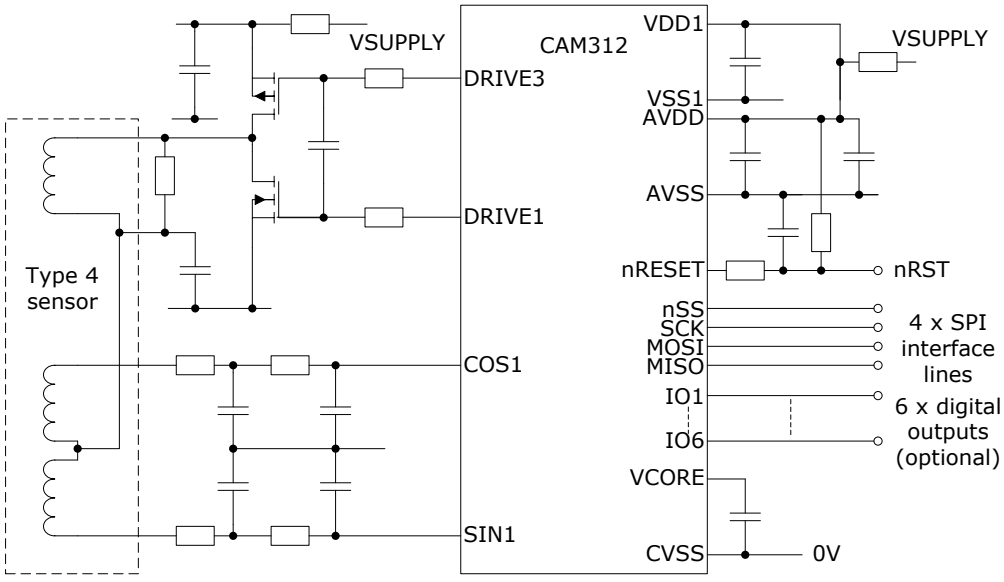

Figure 3 Circuit for reading a single Type 4 sensor

1 CAM312 Functional Description

1.1 Overview

The CAM312 Central Tracking Unit (CTU) chip works with a sensor built from a PCB to measure the position of contactless targets. Targets comprise an inductively coupled resonant circuit. Sensors are available for linear, rotary and arc measurement and in a range of different sizes.

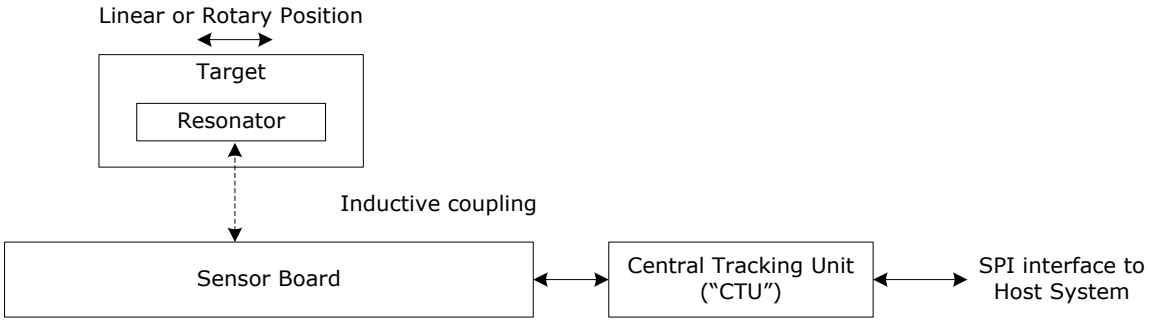

Figure 4 Resonant inductive position sensing system

Sensor Types differ in their details, but the same basic measuring principle applies to them all. The CAM312 chip generates signals that drive external miniature MOSFETs. These, in turn, drive AC current into the sensor's excitation coil. The excitation coil current generates an AC field which powers the resonator at its resonant frequency. The energy in the resonator is built up during this pulse.

Then the current is removed, and the resonator induces decaying EMFs in the sensor coils. The CAM312 chip detects the amplitude of this echo in each sensor coil. It then uses the amplitude values to calculate position.

The details of the measuring process and calculation depend on sensor Type. In all cases, sensing and calculation are fully ratiometric for immunity to changes in amplitude due to gap, misalignment, temperature, target frequency and supply voltage.

The pulse echo interrogation method separates the excitation and detection processes in time. This yields immunity from stray coupling between excitation and sensor coils, and superior sensing performance.

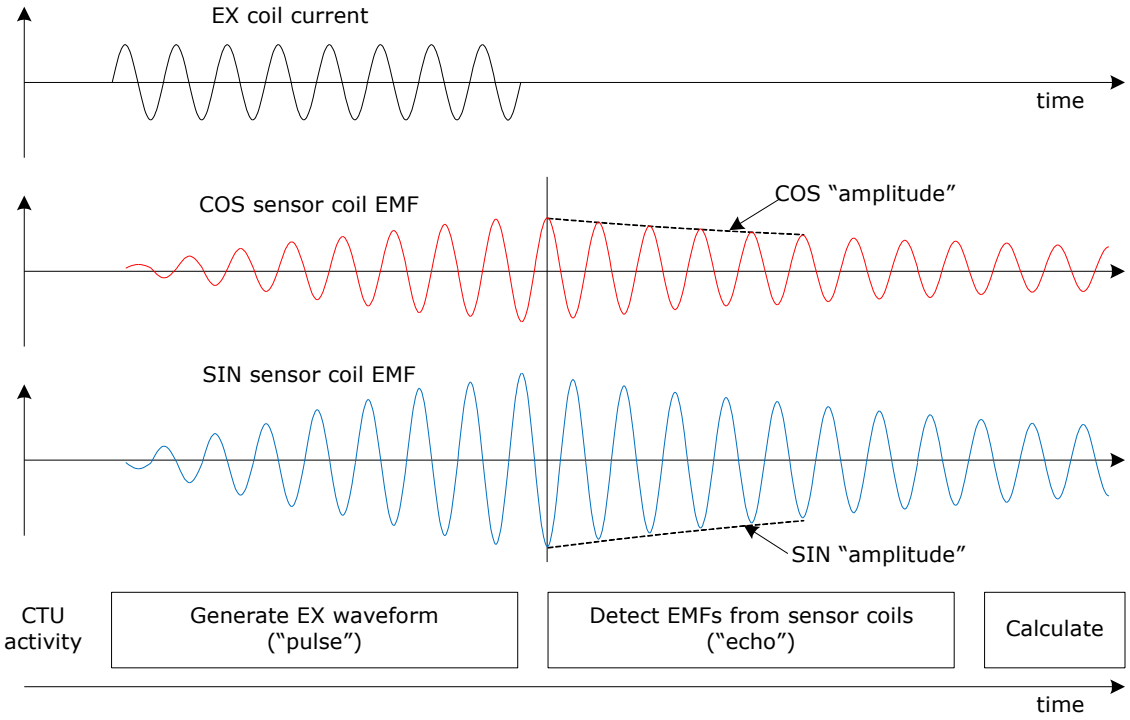

Figure 5 Electronic measuring process

1.2 Sensor Types

Table 1 lists the sensor types currently supported by the CAM312, and includes section references for more details on each Type.

Table 1 Comparison of sensor types

Type	Number of coils in each sensor		Applications	Max number of sensors (CAM312)	Has Subtypes?	Section number for details
	Excitation	Sensing				
4	1	2	Simple linear, rotary and arc sensors	2	No	3
6	1	4	Precision linear and rotary sensors	1	Yes	4
2	1	4	Long precision linear sensors	1	Yes	5

1.3 Pin Names and Functions

Table 2 summarises CAM312 pin functions and type. Please refer to section 2 for electrical characteristics for each type.

Table 2 CAM312 pin names and functions

Signal Name	Type	Function
VDD	Power	Positive supply voltage.
AVDD	Analog Input	Analog supply voltage, connect to VDD.
VSS, AVSS, CVSS	Power	0V connection and common return for sensor inputs
VCORE	Power	On-chip 1.8V regulator decoupling capacitor connection
nRESET	Digital Input	Hardware reset, active low
nSS	Digital Input	SPI Interface line: Slave Select, active low.
SCLK	Digital Input	SPI Interface line: Serial Clock.
MOSI	Digital Input, 5 V Tolerant	SPI Interface line: Master Out, Slave In.
MISO	Digital Output (1)	SPI Interface line: Master In, Slave Out.
IO1, IO2, IO4, IO5, IO6	Digital or Open Drain Output, 5V Tolerant	User configurable IO.
IO3	Digital or Open Drain Output	
DRIVE1 – DRIVE4	Digital Output	Used to drive external MOSFETs for powering the excitation coil of the resonant inductive position sensor
COS1, COS2 SIN1, SIN2	Analog Inputs	Used to sense the sensor coil outputs of resonant inductive sensors.
A0, A1		Do not connect
Pin 4	Not used	Do not connect
Exposed Pad	Shield	Large pad under package. Connect to Vss.

Note (1): MISO is driven as a digital output by the CAM312 during SPI transactions (nSS low), and is Open Drain at other times to allow other slave devices to share the SPI bus.

2 Electrical Characteristics

2.1 Operating Characteristics

Table 3 Operating characteristics

Item	Min	Max	Comments
Operating Supply Voltage VDD, AVDD	3.0V	3.60V	
Operating Temperature	-40˚C	125˚C	Ambient temperature, CAM312ME
Operating Temperature	-40˚C	150˚C	Ambient temperature, CAM312MA
VDD start voltage relative to VSS		0V	For reliable power on reset
VDD rise rate relative to VSS	0.05V/ms		

2.2 Absolute Maximum Ratings

Table 4 Absolute maximum ratings

Item	Max
Voltage between VDD or AVDD and VSS	-0.3V to +4.0V
Voltage on 5V Tolerant pins relative to VSS when VDD≥3.0V	-0.3V to +5.5V
Voltage on 5V Tolerant pins relative to VSS when VDD<3.0V	-0.3V to +3.6V
Voltage on any other pin relative to VSS	-0.3V to (VDD+0.3V)
Current into or out of Digital Output (operating temperature ≤125°C)	4mA
Current into or out of Digital Output (CAM312MA, -40°C to 150°C)	2.5mA

2.3 Digital Input Specifications

Table 5 Digital input specifications

Item	Min	Max
Input Low	VSS	0.2 x VDD
Input High, 5V Tolerant	0.8 x VDD	5.5V
Input High, NOT 5V Tolerant	0.8 x VDD	VDD
Input leakage current		±2µA

2.4 Digital Output Specifications

Table 6 Digital output specifications

Item	Min	Max	Comments
Output Low Voltage		0.4V	IOL = 4mA
Output High Voltage (Digital setting)	2.4V		VDD=3.3V IOH = -4mA
Output High Current (Open Drain setting)		±2µA	
Output High Voltage, Open Drain, 5V Tolerant		5.5V	Maximum allowed
Output High Voltage, Open Drain		VDD	Maximum allowed

2.5 Application Memory Characteristics

Table 7 Application Memory characteristics

Item	Min	Max	Comments
Number of FLASH updates		2000	Across Operating Supply Voltage and Operating Temperature
Characteristic retention, -40°C to +125°C	20 years		

3 Type 4 (and Type 1) Sensor Application

Type 4 sensors include an excitation coil to energise the resonator inside a target, and a single pair of COS/SIN sensor coils to detect the position of the resonator.

This circuitry is also for connecting Type 1 sensors. The only difference is that Type 4 sensors have a common VREF connection for all coils.

3.1 Circuit Schematics, Single Type 4

The circuit for connecting a single Type 4 sensor to the CAM312 chip is shown Figure 6 below. Component values are listed in Table 8.

VCORE is an external connection to an on-chip 1.8V regulator. This pin requires an external decoupling capacitor C_CORE. It must not be connected to other circuitry.

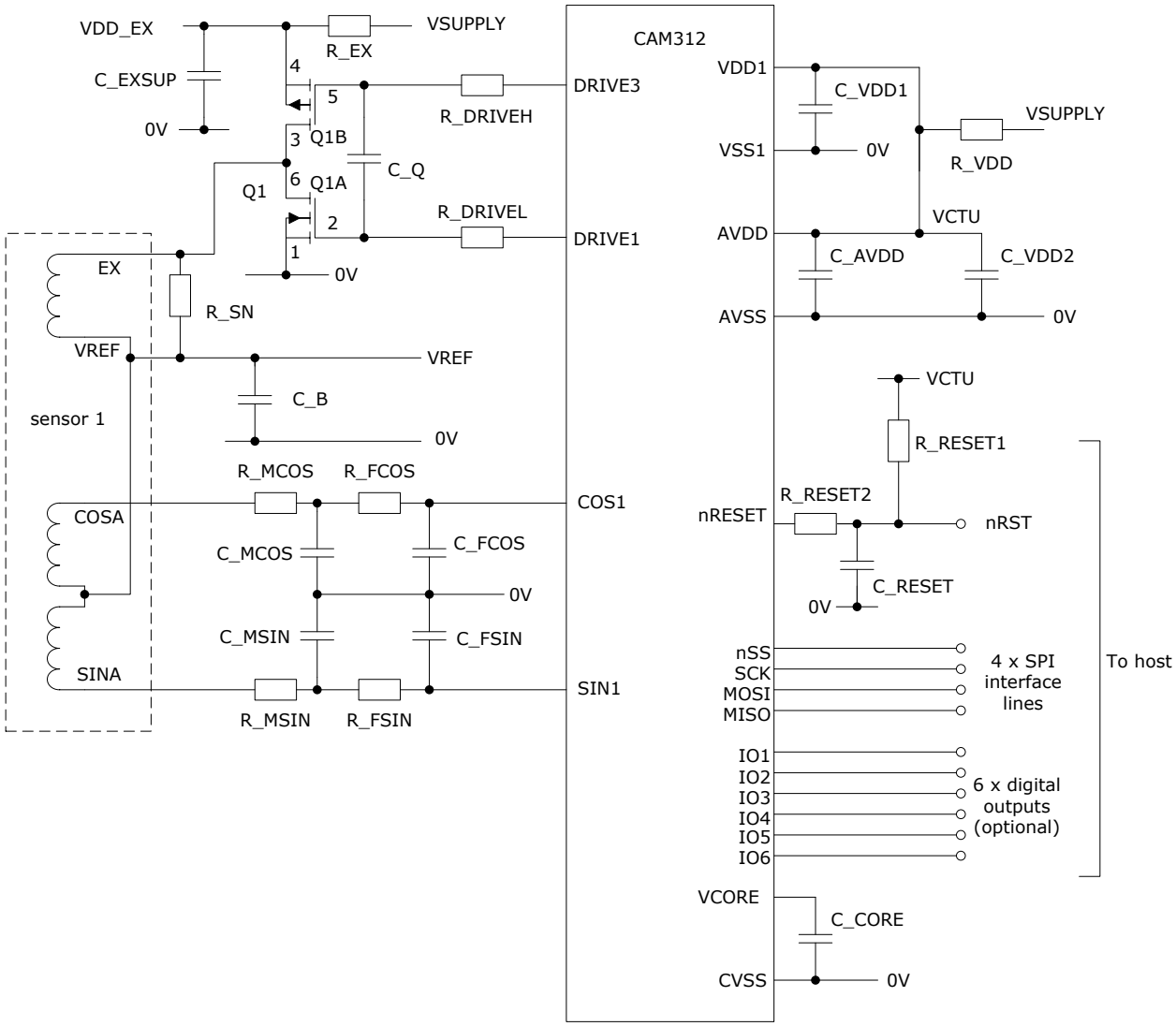

Figure 6 CAM312 connections, single Type 4 sensor

The CAM312's nRESET pin requires a series resistor R_RESET2 for current limiting in the event of ESD, a pull-up resistor R_RESET1 and a reset timing capacitor C_RESET. The host may also perform a reset, by pulling the signal nRST low with an open drain output. Connecting the reset line in this way simplifies bootloader operation.

MISO is an open drain output when nSS is high, and requires a pull-up resistor of 4.7kΩ if this is not provided by the host.

The CAM312 uses an external MOSFET half bridge to drive a Type 4 sensor's excitation coil. MOSFET pair Q1A and Q1B is available as a single miniature device. The gate drive circuit uses 2 resistors and 1 capacitor, and is designed to enable the CTU to drive the bridge output to a high impedance state. The resistors R_DRIVE limit the operating speed of the MOSFETs, to minimise capacitively coupled emissions. The capacitor C_Q prevents excessive shoot-through current during switching. R_SN absorbs the energy in the excitation coil on the transition from low to high impedance. The energy required for each pulse of excitation current is stored in C_EXSUP. R_EX limits the peak charging current.

The sensor's COS and SIN coil inputs have two stages of RC filtering for immunity to external high frequency interference. The reference voltage VREF is generated by the switching action of the MOSFET driver. VREF should not be generated by other means.

3.2 Circuit Schematics, Additional Type 4

The CAM312 chip can process two Type 4 sensors. In this case the circuitry shown in Figure 7 is required in addition to that of Figure 6.

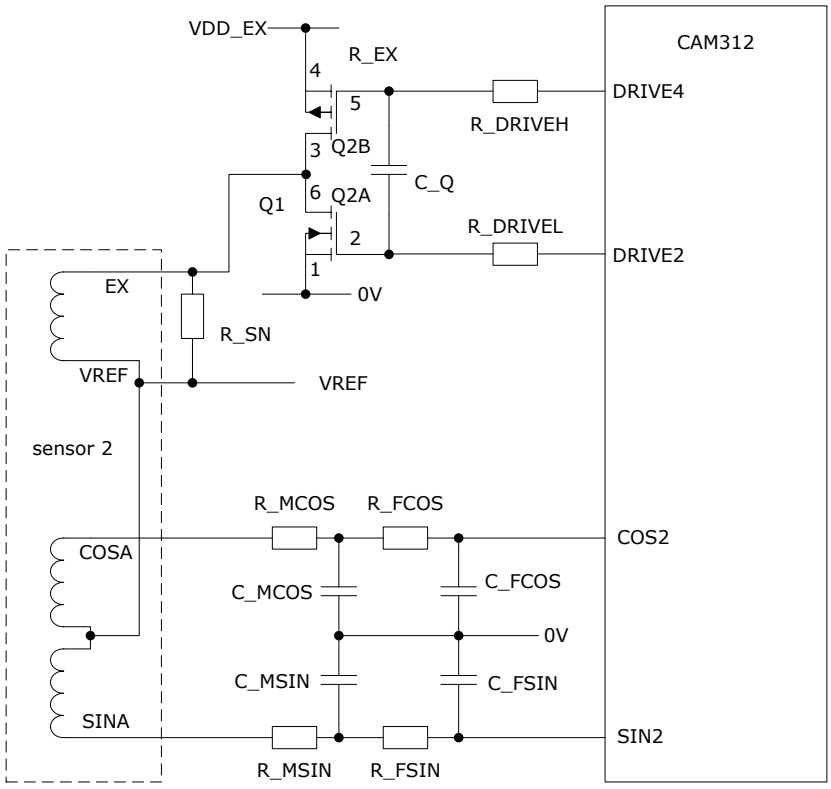

Figure 7 CAM312 connections, additional Type 4 sensor

The second sensor's excitation circuitry shares excitation decoupling capacitor C_EXSUP with the first. It also shares the same capacitor C_B used to establish the bias voltage VREF.

3.3 Components Required, Type 4

Table 8 lists the component values and numbers required for the schematics of Figure 6 and Figure 7.

Table 8 components required for Type 4 sensor connection

Circuit Ref	Value	Tolerance		Number required	
		Grade A	Grade B	1 sensor	2 sensors
R_RESET1	10kΩ	±5%		1	1
R_RESET2	470 Ω	±5%		1	1
R_VDD	1Ω	±5%		1	1
R_EX	4.7Ω	±5%		1	1
R_DRIVEL	1.6kΩ	±5%		1	2
R_DRIVEH	330Ω	±5%		1	2
R_SN	1kΩ	±5%		1	2
R_MCOS/SIN	150Ω	±0.1%	±1%	2	4
R_FCOS/SIN	150Ω	±0.1%	±1%	2	4
C_VDD1, C_AVDD	100nF	±10%		2	2
C_CORE, C_EXSUP, C_VDD2	10µF, ESR < 1 Ω	±20%		3	3
C_RESET	1nF	±10%		1	1
C_Q	1nF	±10%		1	2
C_MCOS/SIN	1nF	±1%	±5%	2	4
C_FCOS/SIN	1nF	±1%	±5%	2	4
C_B	4.7µF	±10%		1	1
Q1 (and Q2 if 2 sensors)	FDY4000CZ			1	2

The value of C_EXSUP may be increased in order to reduce peak supply current, see section 10.11.

The filter components connected to the CAM312 chip 's sensor inputs are important for reproducibility. The table above includes two grades for them: A and B. Grade A yields the least system to system reproducibility error due to component differences. Grade B components are slightly more cost effective. Grade A and B reproducibility error is compared in Table 9.

Table 9 reproducibility error due to filter components, Type 4

Grade	Reproducibility due to filter components (% of Sin Length)
A	±0.04%
B	±0.2%

4 Type 6 Sensor Application

Type 6 sensors are for the precise measurement of rotary and linear position. Their additional precision comes from fine ("A") sensor coils whose signals repeat multiple times along the measuring path. This multiplies resolution and accuracy. Coarse ("B") sensor coils provide full absolute position measurement. The CAM312 chip combines data from both fine and coarse coils to deliver a full absolute position output.

4.1 Circuit Schematics, Type 6

The circuit for connecting a Type 6 sensor to the CAM312 chip is shown in Figure 8Figure 7 below. Component values are listed in Table 10.

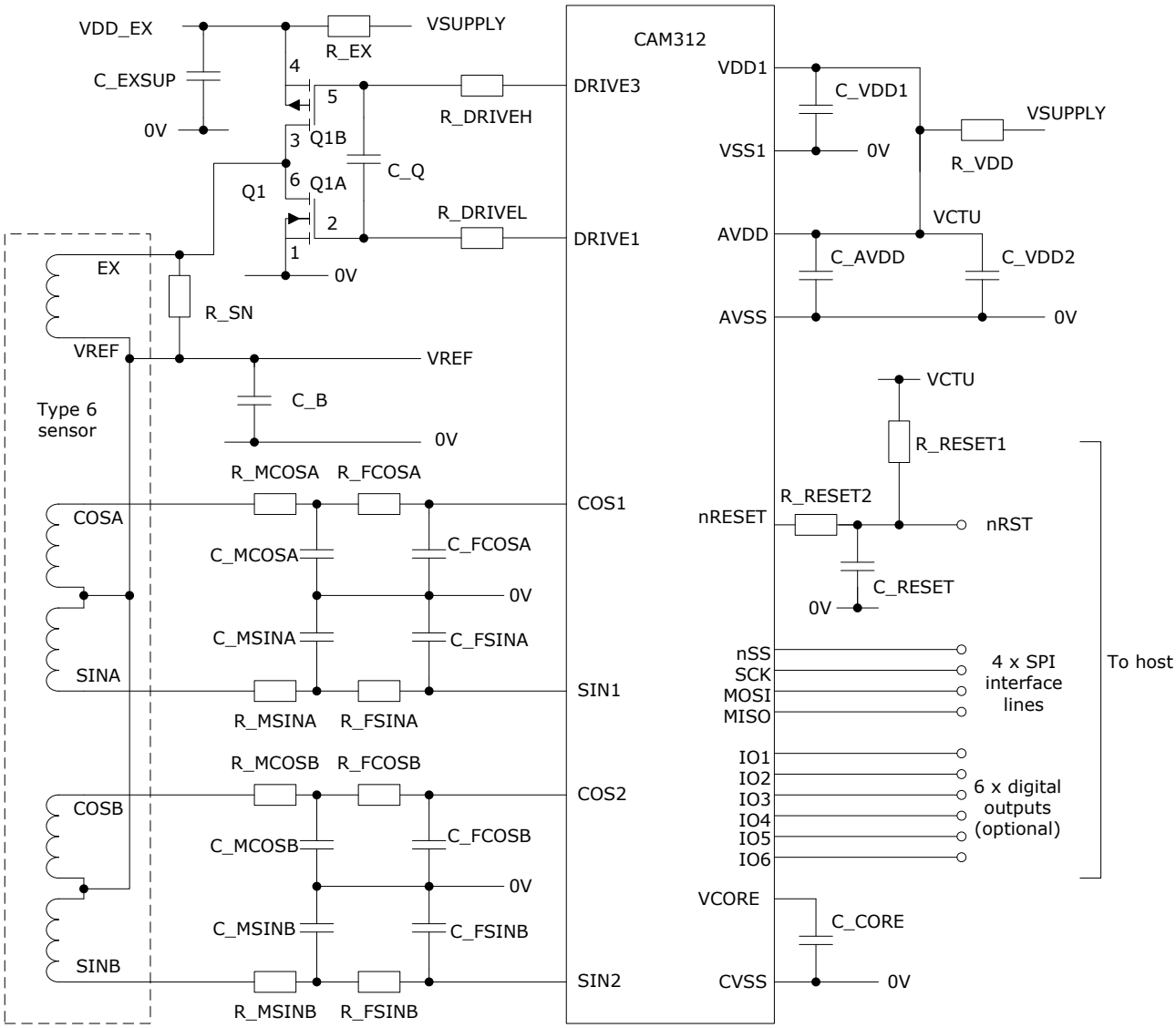

Figure 8 CAM312 connections, Type 6

The circuit design is very similar to that for Type 4 sensors, except for the additional filter components for processing signals from the sensor's coarse sensor coils COSB and SINB. Please refer to section 3.1 for a description of the circuitry.

Note that MISO is an open drain output when nSS is high, and requires a pull-up resistor of 4.7kΩ if this is not provided by the host.

4.2 Components Required, Type 6

Table 10 lists the component values and numbers required for the schematic of Figure 8.

Table 10 components required for Type 6 sensor connection

Circuit Ref	Value	Tolerance		Number required
		Grade A	Grade B	
R_RESET1	10kΩ	±5%		1
R_RESET2	470 Ω	±5%		1
R_VDD	1Ω	±5%		1
R_EX	4.7Ω	±5%		1
R_DRIVEL	1.6kΩ	±5%		1
R_DRIVEH	330Ω	±5%		1
R_SN	1kΩ	±5%		1
R_MCOS/SINA	150Ω	±0.1%	±1%	2
R_FCOS/SINA	150Ω	±0.1%	±1%	2
R_MCOS/SINB	150Ω	±5%		2
R_FCOS/SINB	150Ω	±5%		2
C_VDD1, C_AVDD	100nF	±10%		2
C_CORE, C_EXSUP, C_VDD2	10µF, ESR < 1 Ω	±20%		3
C_RESET	1nF	±10%		1
C_Q	1nF	±10%		1
C_MCOS/SINA	1nF	±1%	±5%	2
C_FCOS/SINA	1nF	±1%	±5%	2
C_MCOS/SINB	1nF	±10%		2
C_FCOS/SINB	1nF	±10%		2
C_B	4.7µF	±10%		1
Q	FDY4000CZ			1

The value of C_EXSUP may be increased in order to reduce peak supply current, see section 10.11.

The filter components connected to the CAM312 chip's sensor inputs are important for reproducibility. The table above includes two grades for them: A and B. Grade A yields the least system to system reproducibility error due to component differences. Grade B components are slightly more cost effective. Grade A and B reproducibility error is compared in Table 11.

Table 11 reproducibility error due to filter components, Type 6

Grade	Reproducibility due to filter components (% of Sin Length)	Reproducibility examples	
		Rotary Type 6.5, SinLength=72°	Linear Type 6.12, SinLength = 31.6mm
A	±0.04%	±0.03°	±0.013mm
B	±0.2%	±0.14°	±0.063mm

Note that only the filter components connecting the fine sensor coils require tighter tolerance components (e.g. R_MCOS/SINA). Filter components connecting the coarse sensor coils do not require tight tolerance because coarse coil errors do not contribute to measurement results.

5 Type 2 Sensor Application

Type 2 sensors are for the precise measurement of linear position. Like Type 6 sensors, their additional precision comes from fine ("A") sensor coils whose signals repeat multiple times along the measuring path. This multiplies resolution and accuracy. Coarse ("B") sensor coils provide full absolute position measurement. The CAM312 chip combines data from both fine and coarse coils to deliver a full absolute position output.

5.1 Circuit Schematics, Type 2

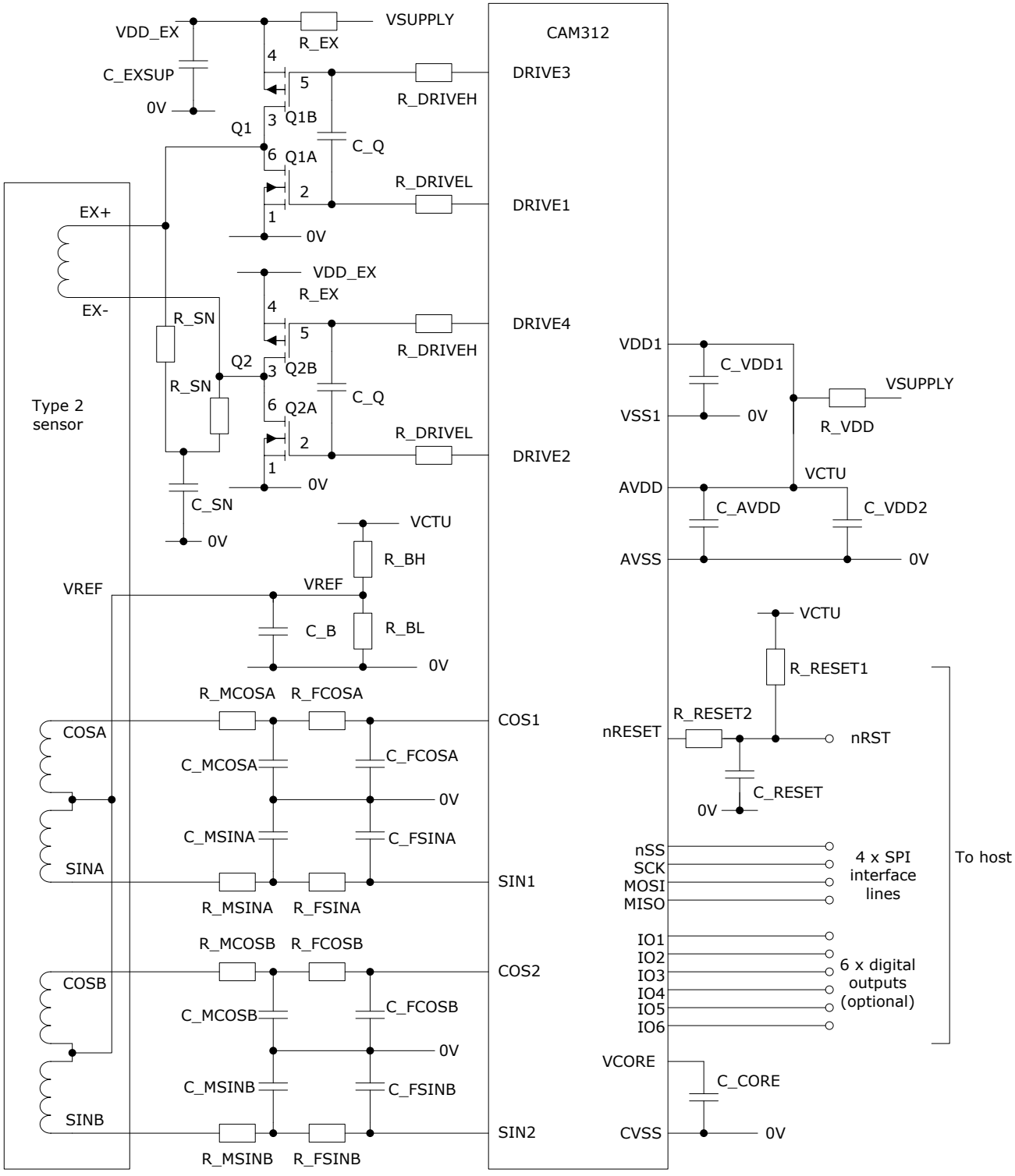

Figure 9 CAM312 connections, Type 2

The circuit for connecting a Type 2 sensor to the CAM312 chip is shown in Figure 9 above. Component values are listed in Table 12.

The difference between Type 2 and Type 6 sensor circuitry is that Type 2 uses a full bridge drive circuit for the excitation coil. This delivers a greater voltage across the excitation coil, allowing it to apply greater power which is generally required for Type 2 sensors due to their larger size.

The full bridge drive circuit comprises MOSFET pairs Q1 and Q2, and their associated gate drive components. The two resistors R_SN and capacitor C_SN absorb the energy in the excitation coil on the H bridge's transition from low to high impedance.

Resistors R_BH and R_BL provide a DC bias voltage VREF for the sensor coil inputs to the CAM312 chip. These bias resistors are not present in Type 4 and Type 6 circuitry. They are required for the Type 2 circuitry because the excitation process does not provide a suitable bias voltage, and the excitation coil does not share decoupling capacitor C_B.

In other respects the circuit design is very similar to that for Type 4 and Type 6 sensors. Please refer to section 3.1 for a description of the circuitry.

Note that MISO is an open drain output when nSS is high, and requires a pull-up resistor of 4.7kΩ if this is not provided by the host.

5.2 Components Required, Type 2

Table 12 lists the component values and numbers required for the schematic of Figure 9.

Table 12 components required for Type 2 sensor connection

Circuit Ref	Value	Tolerance		Number required
		Grade A	Grade B	
R_RESET1	10kΩ	±5%		1
R_RESET2	470 Ω	±5%		1
R_VDD	1Ω	±5%		1
R_EX	1Ω	±5%		1
R_DRIVEL	1.6kΩ	±5%		2
R_DRIVEH	330Ω	±5%		2
R_SN	100Ω	±5%		2
R_MCOS/SINA	150Ω	±0.1%	±1%	2
R_FCOS/SINA	150Ω	±0.1%	±1%	2
R_MCOS/SINB	150Ω	±5%		2
R_FCOS/SINB	150Ω	±5%		2
R_BH, R_BL	10kΩ	±5%		2
C_VDD1, C_AVDD	100nF	±10%		2
C_CORE, C_EXSUP, C_VDD2	10µF, ESR < 1 Ω	±20%		3
C_RESET	1nF	±10%		1
C_Q	1nF	±10%		2
C_MCOS/SINA	1nF	±1%	±5%	2
C_FCOS/SINA	1nF	±1%	±5%	2
C_MCOS/SINB	1nF	±10%		2
C_FCOS/SINB	1nF	±10%		2
C_B	4.7µF	±10%		1
C_SN	10nF	±10%		1
Q1, Q2	FDY4000CZ			2

The value of C_EXSUP may be increased in order to reduce peak supply current, see section 10.11.

The filter components connected to the CAM312 chip's sensor inputs are important for reproducibility. The table above includes two grades for them: A and B. Grade A yields the least system to system reproducibility error due to component differences. Grade B is slightly more cost effective. Grade A and B reproducibility error is compared in Table 13.

Table 13 reproducibility error due to filter components, Type 6

Grade	Reproducibility due to filter components (% of Sin Length)	Reproducibility examples, Linear Type 2.12	
		SinLength=31.2mm	SinLength=50.0mm
A	±0.04%	±0.13mm	±0.02mm
B	±0.2%	±0.063mm	±0.1mm

Note that only the filter components connecting the fine sensor coils require tighter tolerance components (e.g. R_MCOS/SINA). Filter components connecting the coarse sensor coils do not require tight tolerance because coarse coil errors do not contribute to measurement results.

6 Circuit Layout

This section contains recommendations for the PCB layout of the CAM312 circuitry, and applies to Type 4 sensor circuitry (section 3), Type 6 (section 4) and Type 2 (section 5).

6.1 Ground Plane and Capacitor Connections

It is recommended to use a PCB with at least 4 layers, one of which should be a solid ground plane below the CAM312. Conductors carrying signals not associated with the CAM312 chip should not be placed between the CAM312 chip and ground plane.

Connections from the CAM312 chip's VSS, AVSS and CVSS pins to the ground plane must be made with vias placed close to the chip. They should ideally also be connected together to the centre pad. Capacitors C_VDD1, C_AVDD and C_CORE must be kept close to the chip with short distances to ground connections. The same goes for C_B, C_FCOS1 and C_FSIN1, and C_FCOS2 and C_FSIN2 if used. Figure 10 illustrates recommended locations for these components, and their connections. Connections to the CAM312 chip's other pins are less critical.

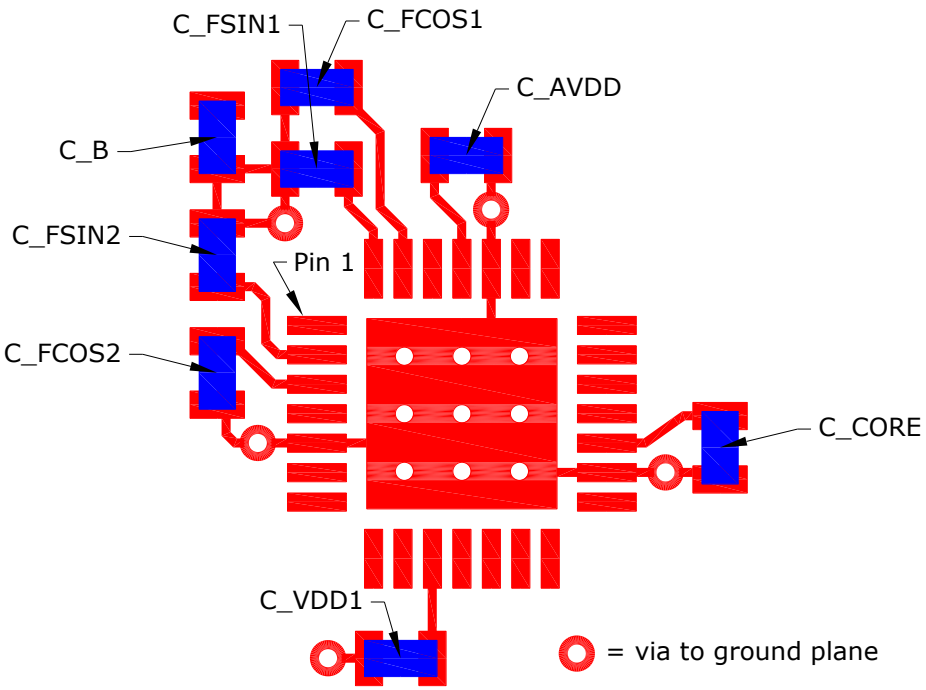

Figure 10 Recommended capacitor locations and wiring

6.2 Sensor Coil and Filter Network Connections

Figure 11 illustrates connections between sensor coils and the CAM312 circuit, including its filter components. When a sensor coil is connected to the CAM312 circuit, the traces and/or wires forming the connection make a loop. The loop formed by the COSA coil (or a Type 4 sensor 1 COS coil) connections is shaded as an example.

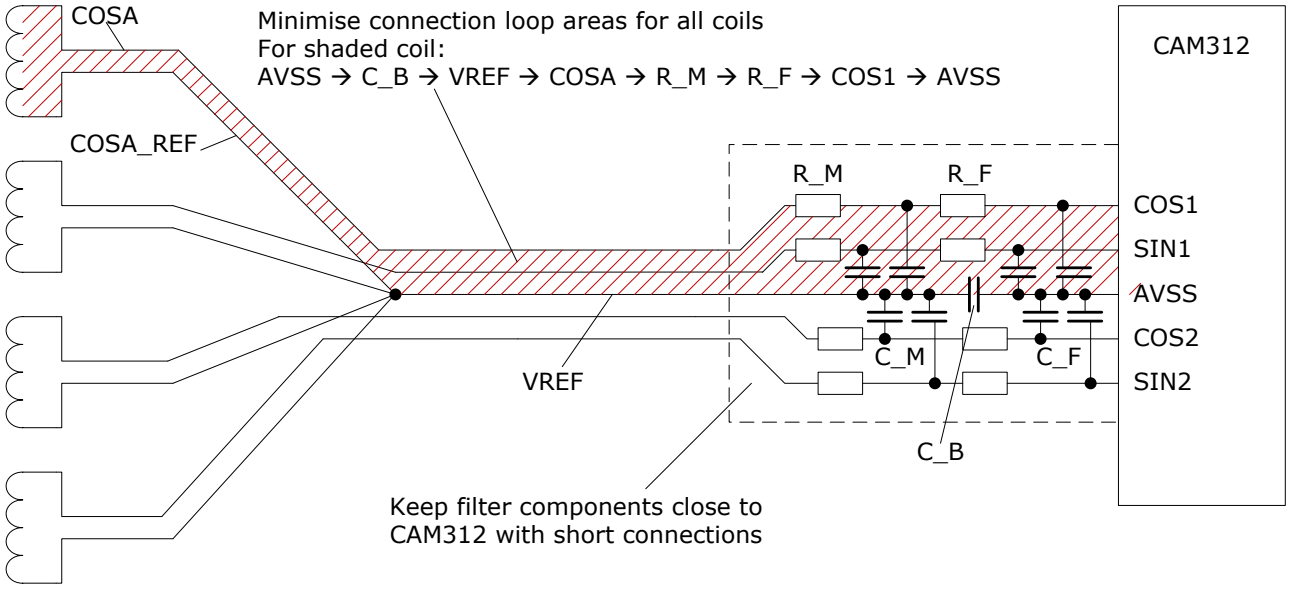

Figure 11 Sensor coil and filter connections to CAM312

The loop area for each of the sensor coils must be minimised, in order to minimise coupling to the target and/or any AC magnetic interference. Wires used for connection must be run in a tight bundle, on adjacent conductors in a ribbon cable or twisted.

Conductors which run for more than 100mm on a PCB should be arranged in coil pairs as in Figure 12 (a) or (b), or adjacent to a common VREF conductor as in Figure 12 (c) or (d).

Shorter conductors may be arranged above or below a ground plane, as in Figure 12 (e). In this case the conductors must avoid the outer 4mm of the ground plane, where the ground plane is less effective at shielding loops against signals from a nearby target and/or AC magnetic interference.

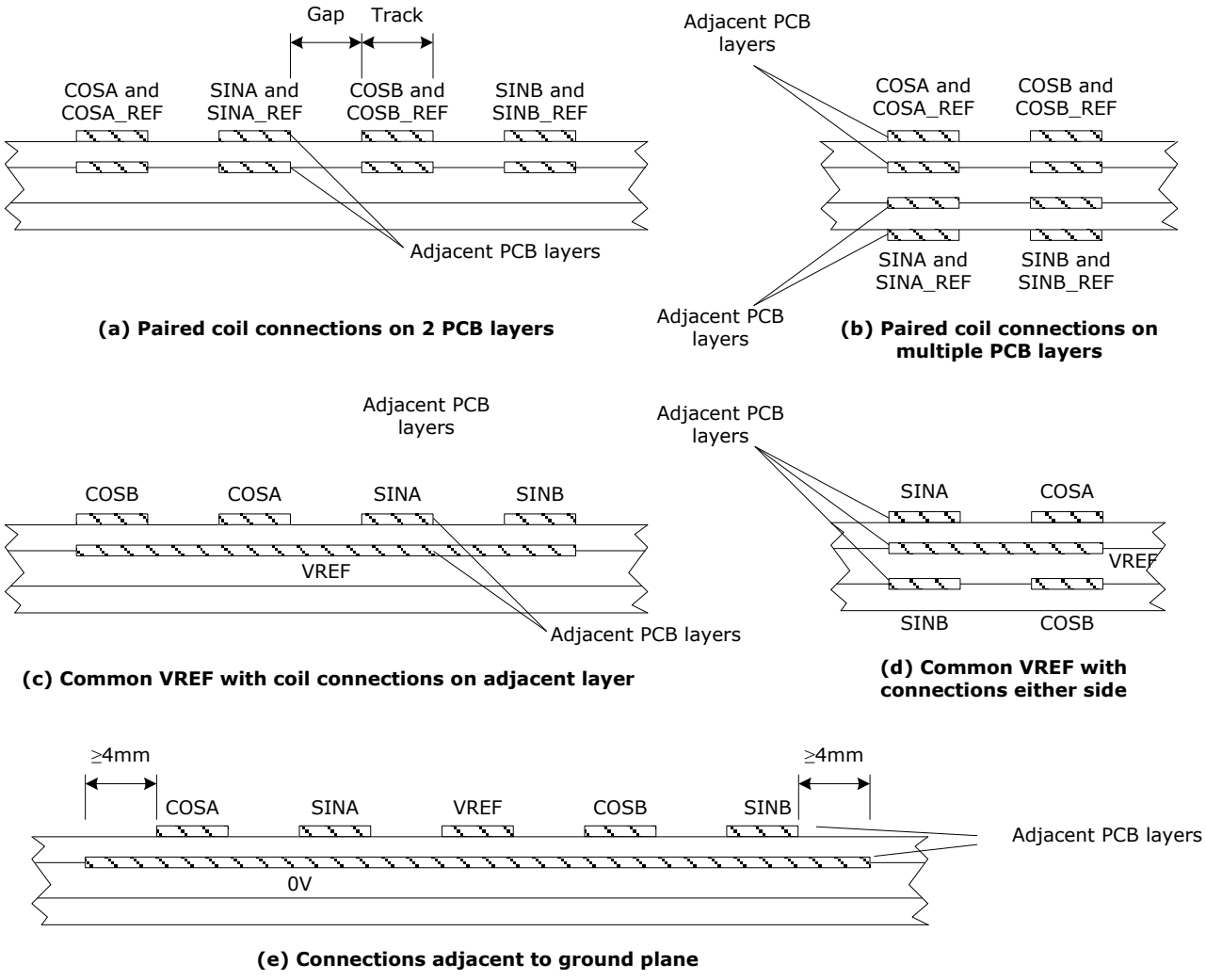

Figure 12 PCB conductor arrangements for sensor coils

Track and Gap figures should be minimised, providing connection resistance does not fall below 5Ω, or below 1Ω for a VREF connection that is common to two or more coils.

6.3 Excitation Circuit and Coil Connections

The CAM312 chip drives the gates of external MOSFET pair(s), which in turn drive current into the excitation coil to energise the resonator inside the target. Type 2 circuitry uses a H-bridge circuit employing two MOSFET pairs, while Type 4 circuitry (Figure 6) and Type 6 circuitry (Figure 8) use a single MOSFET pair.

To keep the circuit efficient and to minimise emissions, the excitation circuit's decoupling capacitor C_EXSUP must be kept close to the MOSFET pair(s), and should be connected to them with fat traces and the minimum of trace lengths.

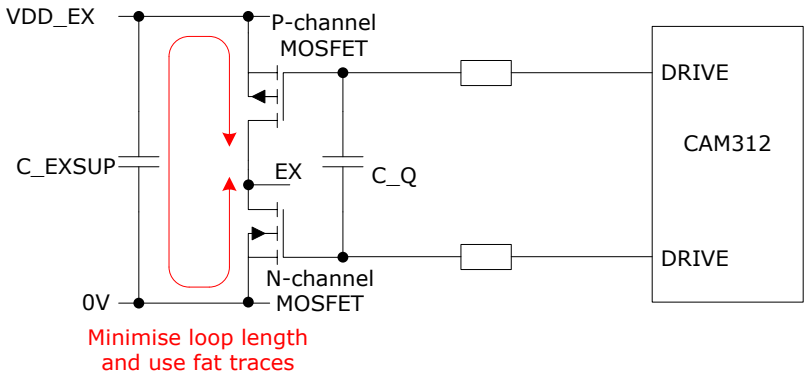

Figure 13 Excitation circuit layout

Each capacitor C_Q should be located near the MOSFET it is connected to.

Excitation coil connections must be made with a minimum of loop area, in a similar way to sensor coil connections.

The excitation coil connecting track widths should preferably be wide to minimise resistance. A loop resistance of less than 0.5Ω is preferable. PCBs with 1oz copper (34µm thick) have a surface resistivity of 0.5mΩ/square, so connections can be up to 1000 squares long. Table 14 shows how the minimum width of each trace in the pair of traces connecting the excitation coil varies with length.

Sensor and excitation traces may be run adjacent to one another. Type 4 and Type 6 sensors share a common VREF for both sensor and excitation coil, and the EX connection may be added to one side of the parallel connections shown in Figure 12 (c) or (d). It is more important to minimise sensor coil connection area than excitation, in any case that there is a conflict between the two.

Table 14 Minimum conductor widths on 1oz (34µm) PCB for ≤ 0.5Ω loop resistance

Length of excitation conductor pair	Minimum conductor width
100mm	0.2mm
200mm	0.4mm
400mm	0.8mm
800mm	1.6mm

7 Resonator Detection

7.1 Background

The CAM312 chip may be connected to different sensor types as described in the preceding sections. In each case the sensor couples with a moving target to measure its position. The coupling is inductive (AC magnetic fields). The target includes an electrical resonator comprising an inductor ("L") and capacitor ("C"). The system is illustrated in Figure 14.

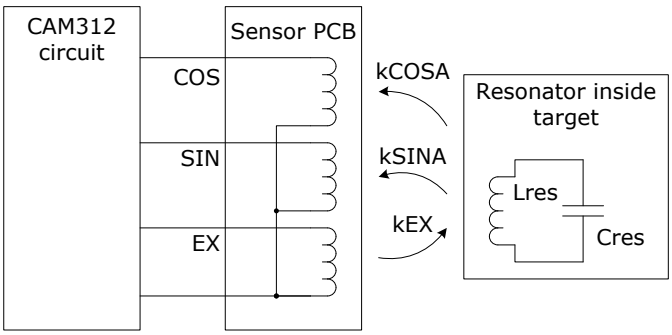

Figure 14 CAM312 connected to sensor coupled with resonator in target

A resonator can be characterized with two parameters: its resonant frequency "Fres" and quality factor "Q". The resonant frequency is the frequency of the resonance illustrated in Figure 5. The Q is a measure of how fast the resonance decays. Resonant inductive sensors generally return higher signal levels and work better with higher Q values, corresponding to slower decay.

The CAM312 chip energises the excitation coil to power the resonator at its resonant frequency, and then listens to the resulting fields in the COS and SIN senor coils. This process is described in section 1.1. The CAM312 chip is designed to lock onto and track the resonant frequency of inductively coupled resonators inside targets. The CAM312 chip measures the position of each sensor's target in turn. Each time, it also estimates its resonant frequency, providing there is sufficient signal amplitude. If the resonant frequency changes, the CAM312 chip changes its excitation frequency to match. Following power on reset, or if the previous measurement was invalid, the CAM312 chip searches its tuning range for the target. Each measurement the CAM312 tries a different frequency until it achieves lock. This means it can take a few measurements before the CAM312 reports VALID for any sensor, as specified in Table 15.

Sensors and their targets are described in separate datasheets. Some targets include a prepackaged resonator, for example CambridgeIC's Standard Target part 013-1005. Other sensors work with targets that customers can build themselves, from inductors and capacitors. In this case the resonant frequency is given by Equation 1

Equation 1 Resonant Frequency

$$Fres = \frac{1}{2\pi\sqrt{Lres \times Cres}}$$

The inductor value Lres may be the value of a single inductor, or it may comprise two or more inductors connected together as in a "Type 6 Through Hole Rotary Sensor".

If the target and resonator are well away from metal and magnetic material then they are said to be in "free space". If not, the inductor value Lres may be modified by the presence of the material, and the resulting value of Fres will be similarly modified according to Equation 1. When designing targets and their resonators for use with the CAM312 chip, it is always the actual resonant frequency "seen" by the CAM312 chip that matters, taking into account the effect of metal and any magnetic material nearby.

The CAM312 chip is designed to work with resonators across a wide frequency range. This means that the effect of nearby metal and magnetic materials is easy to budget for, and that capacitor and inductor tolerances can easily be accommodated. When considering the effects of inductor and capacitor tolerances, the differential of Equation 1 is useful…

Equation 2 Change in resonant frequency due to inductor and capacitor changes

$$\frac{\Delta Fres}{Fres} = -0.5 \times \left(\frac{\Delta Lres}{Lres} + \frac{\Delta Cres}{Cres}\right)$$

For example if Lres has a tolerance of ±3% and Cres a tolerance of ±5%, the resulting tolerance of Fres is ±4%.

For more on frequency tolerances and selection of appropriate resonant frequency and tolerances, please refer to the CambridgeIC white paper "Resonant Frequency Centering".

7.2 Resonator Detection Specifications

Table 15 lists parameters relevant to the CAM312 chip's detection of resonators, and their values.

Table 15 Resonator Detection Specifications

Parameter	Value	Comment
Nominal Resonator Centre Frequency	187.5kHz	For a reported relative frequency of 0Hz with a nominal CAM312 chip
Resonator tuning range Relative to Nominal Resonator Centre Frequency	±10%	Across Operating Temperature Range -40°C to +125°C
	±11%	Across Operating Temperature Range -40°C to +150°C
Minimum Resonator Q-factor	50	For reliable position and frequency detection
Minimum Amplitude	500	For reliable position and frequency detection
	1000	Recommended minimum for design purposes
Maximum number of measurements on a sensor with in-range target before VALID	9	Following a reset or resonator out of range

8 SPI Hardware

8.1 Overview

This section describes how data is written to, and read back from, the CAM312 chip, over its SPI interface. For communication with a host system, the CAM312 chip is always an SPI slave. All communication is initiated by the host.

There are two types of SPI transaction: a Register Access SPI and Checksum Access SPI. A Register Access SPI accesses one or more of the CAM312 chip's internal registers. It may either read or read-write the register(s). A Checksum Access SPI provides a checksum of the previous Register Access SPI's data, to assist with SPI error detection.

8.2 Data Transfer Method

The CAM312 chip always operates as an SPI slave device. The host device starts a data transfer by driving nSS low. It sends data to the CAM312 with the MOSI line, and provides the CAM312 with a serial clock line SCK. The CAM312 detects each MOSI bit on the rising edge of SCK. The CAM312 chip sends data back to the host with the MISO line. Bits change state on the falling edge of SCK, and the host should detect the state of MISO on each rising edge. This is commonly referred to as SPI Mode 0. The beginning and end of an SPI transaction is illustrated in Figure 15.

All SPI transactions MUST be bounded by the Slave Select (nSS) line being driven low at their start and being driven high at their end. The SPI interface will not function if nSS is tied permanently low.

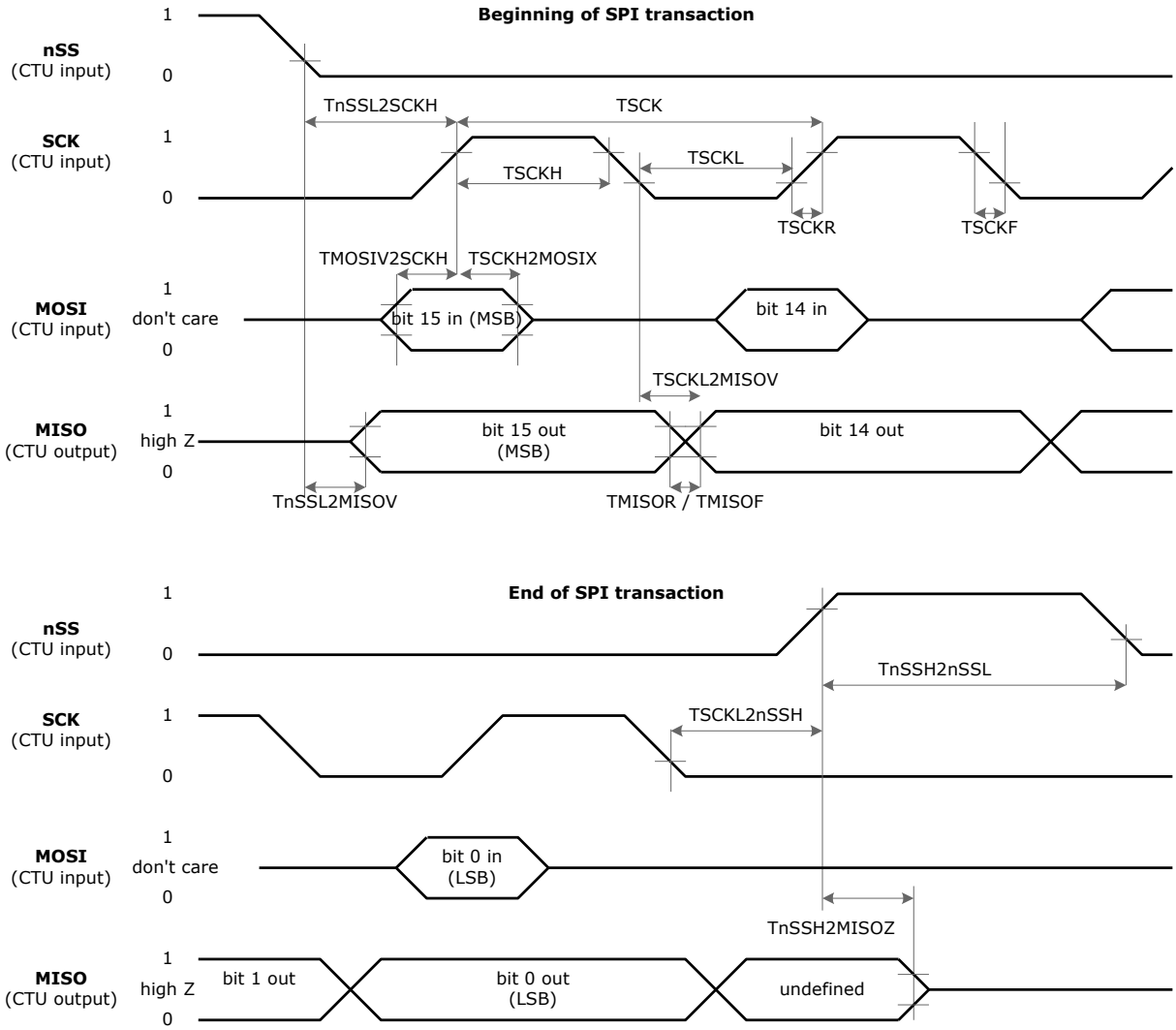

Figure 15 SPI Data Transfer

The timing parameters defined in this section apply to both Register Access SPI transactions and Checksum Access SPI transactions.

8.3 Register Access SPI

The host operates the CAM312 chip by writing to and reading from registers. There are a number of registers with different functions. Each register is 16 bits wide, and has its own 12 bit address.

The host must start each SPI transaction by clocking out 4 ACS bits field followed by 12 address bits on MOSI. The function of the ACS bits is defined in Table 14. The ACS bits define whether the current SPI transaction reads from registers (Read), or writes and reads data (Write Read).

Table 16 ACS bits definition

ACS[3:0]	Abbreviation	Access type
0x0	RS	Read
0xF	WRS	Write Read

When the host requests a Read, the next 16 bits clocked out of MISO after the address are the data contained in the register at the specified address. The CAM312 ignores the state of MOSI during data transfer. This transaction is illustrated in Figure 16.

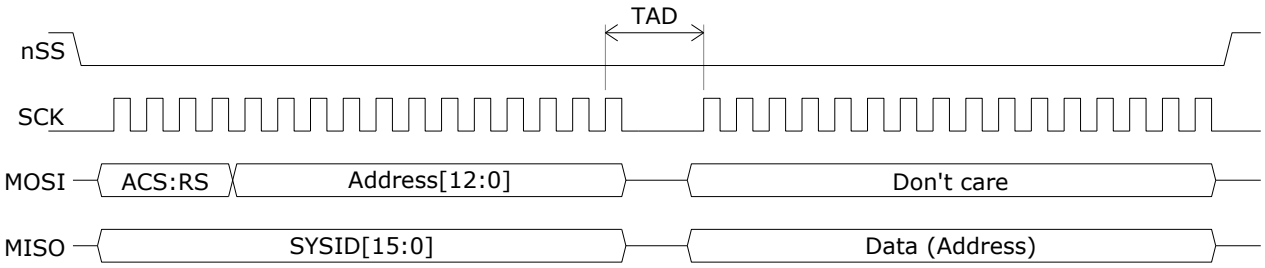

Figure 16 Read, single register

A Write Read operation is similar, except the host also updates the register contents with the new data that the host clocks out of the MOSI line after the address. The data returned on the MISO line is the register contents before the update. This transaction is illustrated in Figure 17.

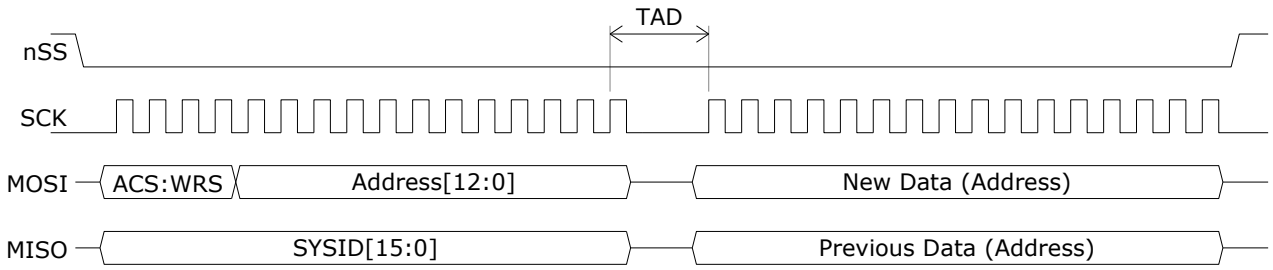

Figure 17 Write Read, single register

For both of these Register Access SP operations, a time TAD is required between the rising edge of SCK that clocks in the last address bit and the rising edge of SCK that clocks out the first data bit, illustrated in Figure 16 and Figure 17 above. TAD allows the CAM312 time to load its SPI transmit buffer with data from the correct address. This ensures that MISO data is available to the host before the next rising edge of SCK. Different minimum values apply depending on whether or not a measurement is in progress.

If a Register Access SPI transaction is being performed when a measurement is in progress, the required value of TAD is longer to allow the CAM312 to complete measurement tasks which are assigned a higher priority than handling SPI. A measurement is in progress if any sensor is set for continuous measurement (SCW:CONT=GO=1), or if a measurement has been started on any sensor (SCW:GO=1) and not yet finished (sample indicator still clear).

The CAM312 chip outputs the contents of its SYSID register as the first word of each Register Access SPI transaction. This defaults to 0xABCD, and may be changed by the host (section 9.8). Other values are possible when operating in

Bootloader mode, or as a result of errors (see section 10.10). It is recommended that the host checks the SYSID value read back against the expected value as a test for SPI communication integrity.

Instead of accessing a single register, the host may access a set of consecutive registers by extending the SPI transaction as illustrated in Figure 18. Data is transferred one register at a time, starting at the first specified address. Figure 18 illustrates a Multiple Write Read SPI transaction with the host providing ACS, address and new register data with the MOSI signal.

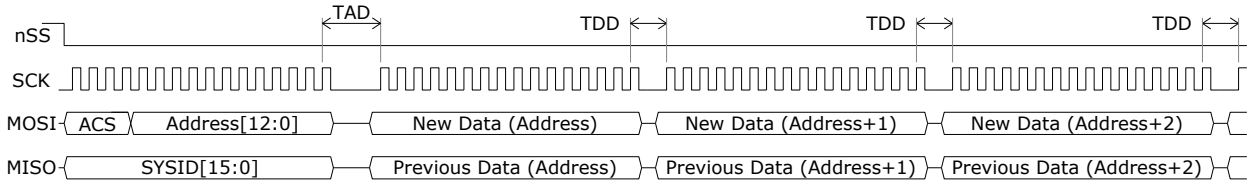

Figure 18 Multiple Register access

A Multiple Read SPI is similar. In this case, though, the host only provides the relevant ACS and address. Once the last address bit has been clocked into the CAM312, the state of MOSI does not matter for the remainder of the SPI transaction and is ignored by the CAM312.

Registers are arranged in blocks dedicated to system functions, and to each sensor connected, distinguished by the upper 4 bits of the address. Multiple register access must not span different blocks. It may only span either system registers or registers associated with a single sensor.

It is not essential to transfer complete 16 bit words into the CAM312. However it is recommended, since data from any incomplete word will be discarded.

Figure 18 defines SPI timing parameter TDD. TDD is measured between the last positive going edge of SCK of one data word to the first positive going edge of SCK of the next data word. The host must ensure that the TDD value it generates is greater than the minimum values specified in Table 17. Different minimum values apply depending on whether or not a measurement is in progress.

When the period of the host's SCK signal (TSCK) is shorter than TDD, pauses in the SCK signal are visible at data word boundaries, as illustrated in Figure 18. It is also possible for the SCK signal to run continuously without pauses, as illustrated in Figure 19. In this case the SCK clock period TSCK must exceed the specified value of TDD(min).

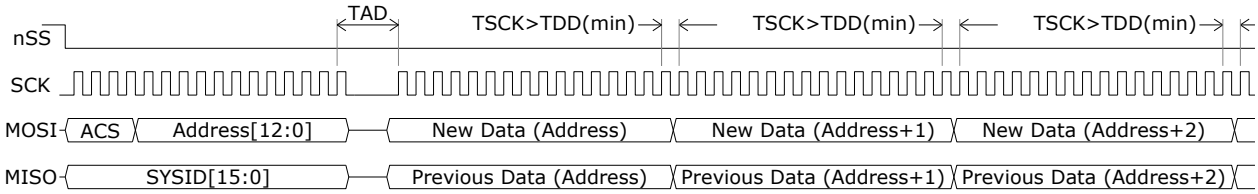

Figure 19 No pauses in SCK signal at data word boundaries

A minimum time is required between Register Access SPI transactions. This allows time for the CAM312 to perform any necessary reconfiguration before the next Register Access SPI occurs. This time is denoted TnSSHR2nSSLR and is illustrated in Figure 20.

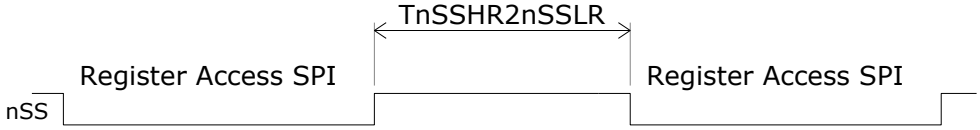

Figure 20 Time TnSSHR2nSSLR requirement

8.4 Timing of IO Changes Following a Register Access SPI

The host may clear a sensor's active Sample Indicator by writing 0 to the sensor's SIF bit in a write read transaction including the SCW register. The state of any User IO mapped to that Sample Indicator will change shortly after the end of the transaction, at a time TnSSH2IOclr defined in Figure 21. The maximum value of this timing parameter is specified in Table 17.

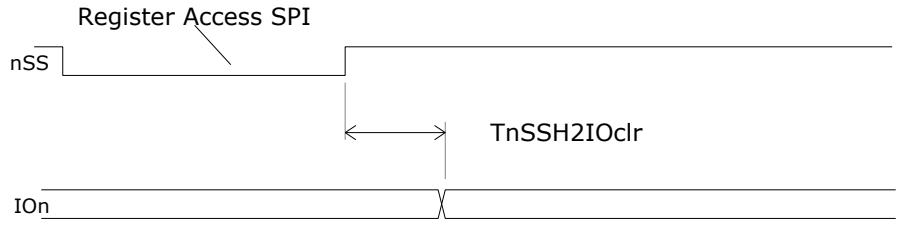

Figure 21 IO Change Following a Register Access SPI

Writes to the SYSIO or SIC registers may also change the state of one or more User IOs. If there is no measurement in progress, the maximum time to change to the new IO states is TnSSH2IOfn(max). This is measured from the end of the SPI transaction, like TnSSH2IOclr. If there is a measurement in progress the IO states may not change until after that measurement.

8.5 Checksum Access SPI

The CAM312 chip calculates a checksum of each Register Access SPI transaction's data. This may be read out immediately after each Register Access SPI transaction.

Reading the checksum is optional. If a checksum is not required, the host should ensure the SPI nSS line is held high for at least TnSSHR2nSSLR(min) after the SPI transaction. Please see Table 17 for the value of this timing parameter.

The CAM312 uses the timing between SPI transactions to distinguish between a Register Access SPI transaction and Checksum Access SPI transaction. If the nSS high time following a Register Access SPI transaction is between TnSSHR2nSSLC(min) and TnSSHR2nSSLC(max), then the then the following SPI is a Checksum Access SPI transaction. TnSSHR2nSSLC is illustrated in Figure 22 below. The minimum value depends on whether or not a measurement is in progress, defined in the same way as for TAD in section 8.3.

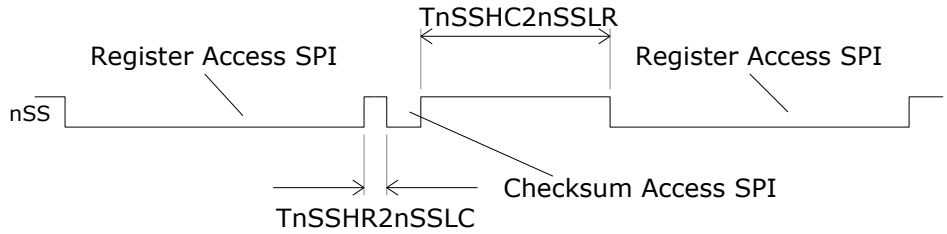

Figure 22 Time TnSSHR2nSSLC requirement

Note that TnSSHR2nSSLC(max) is less than TnSSHR2nSSLR(min), to help the CAM312 to make a clear distinction between Register Access SPI transactions and Checksum Access SPI transactions.

Once the host has read out all 16 bits of the checksum in a Checksum Access SPI transaction, it must take the nSS SPI signal high again. The nSS signal must remain high for at least a time TnSSHC2nSSLR(min) before going low again for the next Register Access SPI transaction. TnSSHC2nSSLR is defined in Figure 22 and specified in Table 17.

The checksum value is obtained by applying a CRC-16 algorithm to the MISO data output by the CAM312 in the preceding Register Access SPI transaction. That is, all complete data words which the CAM312 outputs on MISO, including the first word (SYSID) and the register contents which follow. When a checksum is required, the maximum length of the preceding Register Access SPI transaction is 16 words (SYSID plus 15 data words). The CRC algorithm is summarised in Equation 3, using standard shorthand notation.

Equation 3 CRC-16 Checksum

$$CRC\ Polynomial: x^{16} + x^{15} + x^2 + 1\ (0x8005)$$
$$CRC\ Initialisation: 0x0000$$

8.6 Interface Timing Specifications

Table 17 specifies values for the SPI timing parameters defined in preceding subsections.

Table 17 Interface timing specifications

Parameter	Description		Min	Max	Units
TVALIDCHECK	Time for internal validity checks following reset		5	16	ms
TSCKL	SCK Input Low Time		30	-	ns
TSCKH	SCK Input High Time		30	-	ns
TSCK	SCK clock period		90	-	ns
TSCKR	SCK Input Rise Time		-	10	ns
TSCKF	SCK Input Fall Time		-	10	ns
TMISOR	MISO Rise Time (50pF load)		-	10	ns
TMISOF	MISO Fall Time (50pF load)		-	10	ns
TMOSIV2SCKH	MOSI Setup Time		30	-	ns
TSCKH2MOSIX	MOSI Hold Time		30	-	ns
TnSSL2MISOV	First MISO state valid after nSS low edge		-	80	ns
TSCKL2MISOV	MISO state valid after SCK low edge		-	20	ns
TnSSL2SCKH	nSS low to SCK edge		120	-	ns
TSCKL2nSSH	Last SCK edge to nSS high		90	-	ns
TnSSH2MISOZ	nSS high to MISO high Z		-	100	ns
TAD	Address end to first data	Measurement not in progress (1)	3	-	µs
		Measurement in progress (2)	8	-	µs
TDD	Delay between data words	Measurement not in progress (1)	0.24	-	µs
		Measurement in progress (2)	1.2	-	µs
TnSSHR2nSSLR	Time between end of one Register Access SPI and the beginning of the next		30	-	µs
TnSSHR2nSSLC	Window after SPI to read checksum	Measurement not in progress (1)	3	19	µs
		Measurement in progress (2)	8		µs
TnSSHC2nSSLR	Time between end of Checksum Access SPI and the next Register Access SPI		30	-	µs
TnSSH2IOclr	Time to clear sample indicator following an SPI that cleared it		-	25	µs
TnSSH2IOfn	Time to change IO function following SPI accessing SYSIO or SIC, measured from end of SPI or any measurement in progress		-	30	µs

Operation according to sections 10.3, 10.4 or 10.5 ensures there is no measurement in progress during the SPI transaction. This allows the host to operate with minimum SPI timings, marked (1) in Table 17. To use these timings, the host must not perform any SPI transactions between setting any sensor's GO bit to 1 and that sensor's measurement completing, either indicated by the activation of that sensor's sample indicator or by waiting for the appropriate Minimum Measurement Time specified in Table 28.

The host must use longer SPI timings if the CAM312 may be performing a measurement at the same time as the SPI transaction, marked (2) in Table 17. These longer SPI times are essential in continuous mode (any sensor's SCW:CONT bit set to 1, as in section 10.6). The extra time allows the CAM312 chip to perform measurement functions and respond to SPI activity at the same time.

8.7 Total SPI Transaction Times

Table 18 is a guide to achievable SPI timings. Timing parameters are based on a host operating with fast SPI parameters including a bit rate of 10Mbit/s. The timing parameters selected are close to the minimum values of Table 17, but also allow for typical host tolerances and implementation.

Table 18 Register Access SPI transaction time examples

SPI timings	Registers Accessed	SPI transaction time
TSCK = 100ns (“10Mbit/s”) TnSSL2SCKH = 200ns TAD = 3µs (measurement not in progress) TDD = 300ns SCKL2nSSH = 200ns	SCW, PTEF, RESA, RESB, RESC (Type 4 results)	14µs
	SCW, PTEF, RESA, RESB, RESC, RESD, RESE, RESF (Type 2 or 6 results)	20µs

9 Register Description

The host configures and controls the CAM312 chip by writing to its internal registers. It obtains status and measurement results by reading back from internal registers. This section describes the function of each of the CAM312 chip's registers.

Reading and writing to registers is done over the SPI interface, using the procedures described in section 8. Section 10 describes how to control the CAM312 chip to perform sensor position measurements.

The CAM312 chip's register map is arranged in distinct sections: a system control section and one section for each sensor. The arrangement is illustrated in Figure 23 and Figure 24.

The register map includes a number of registers whose functions are not implemented in the CAM312, for compatibility with other CTU chips. For example the PTEF register controls position trigger behaviour in the CAM204 chip, but is not used in the CAM312.

The register map has been arranged to reduce SPI overheads once the whole system has been initialised following a reset. Once initialised, the host system will normally only need to access a small contiguous block of registers to control each sensor, which can be performed within a single SPI transaction.

	Address	Register
SENSOR 2	0x 2 1F	PTP8
	0x 2 1E	PTP7
	0x 2 1D	PTP6
	0x 2 1C	PTP5
	0x 2 1B	PTP4
	0x 2 1A	PTP3
	0x 2 19	PTP2
	0x 2 18	PTP1
	0x 2 17	PTAH
	0x 2 16	PTC87
	0x 2 15	PTC65
	0x 2 14	PTC43
	0x 2 13	PTC21
	0x 2 12	SIC
	0x 2 11	STYPE
	0x 2 10	DACCW
	0x 2 0F	DACLIMY
	0x 2 0E	DACLIMX
	0x 2 0D	DACPOSD
	0x 2 0C	DACPOSC
	0x 2 0B	DACPOSB
	0x 2 0A	DACPOSA
	0x 2 09	LEDCW
	0x 2 08	CONST
	0x 2 07	RESF
	0x 2 06	RESE
	0x 2 05	RESD
	0x 2 04	RESC
	0x 2 03	RESB
	0x 2 02	RESA
	0x 2 01	PTEF
	0x 2 00	SCW

	Address	Register	Description
SENSOR 1	0x 1 1F	PTP8	Pos Trig Position 8
	0x 1 1E	PTP7	Pos Trig Position 7
	0x 1 1D	PTP6	Pos Trig Position 6
	0x 1 1C	PTP5	Pos Trig Position 5
	0x 1 1B	PTP4	Pos Trig Position 4
	0x 1 1A	PTP3	Pos Trig Position 3
	0x 1 19	PTP2	Pos Trig Position 2
	0x 1 18	PTP1	Pos Trig Position 1
	0x 1 17	PTAH	PT Auto-Clear & Hysteresis
	0x 1 16	PTC87	Position Trigger 8&7 Control
	0x 1 15	PTC65	Position Trigger 6&5 Control
	0x 1 14	PTC43	Position Trigger 4&3 Control
	0x 1 13	PTC21	Position Trigger 2&1 Control
	0x 1 12	SIC	Sample Indicator Control
	0x 1 11	STYPE	Sensor Type
	0x 1 10	DACCW	DAC Control Word
	0x 1 0F	DACLIMY	DAC Limit Y
	0x 1 0E	DACLIMX	DAC Limit X
	0x 1 0D	DACPOSD	DAC Position D
	0x 1 0C	DACPOSC	DAC Position C
	0x 1 0B	DACPOSB	DAC Position B
	0x 1 0A	DACPOSA	DAC Position A
	0x 1 09	LEDCW	LED Control Word
	0x 1 08	CONST	Sensor Constants
	0x 1 07	RESF	Result Register F
	0x 1 06	RESE	Result Register E
	0x 1 05	RESD	Result Register D
	0x 1 04	RESC	Result Register C
	0x 1 03	RESB	Result Register B
	0x 1 02	RESA	Result Register A
	0x 1 01	PTEF	Pos Trig Enables/Flags
	0x 1 00	SCW	Sensor Control Word

System	0x 0 0F	SYSID	Device ID
	0x 0 0E	SYSVER	System Version Number
	0x 0 0D	BOOTVER	Bootloader Version Number
	0x 0 0C	SAVEKEY	Save Key
	0x 0 0B		System Identity
	0x 0 0A		(Reserved)
	0x 0 09		(Reserved)
	0x 0 08		(Reserved)
	0x 0 07		(Reserved)
	0x 0 06		(Reserved)
	0x 0 05		(Reserved)
	0x 0 04		(Reserved)
	0x 0 03	SYSDAC	System DAC Register
	0x 0 02	SYSIO	IO Pin Types
	0x 0 01	SYSI	Continuous Sample Interval
	0x 0 00	SYSCW	System Control Word

Figure 23 Register Map Overview

	Address	Description	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SENSOR 1	0x 1 1F	Pos Trig Position 8	PTP8	PTP8 [15:0]															
	0x 1 1E	Pos Trig Position 7	PTP7	PTP7 [15:0]															
	0x 1 1D	Pos Trig Position 6	PTP6	PTP6 [15:0]															
	0x 1 1C	Pos Trig Position 5	PTP5	PTP5 [15:0]															
	0x 1 1B	Pos Trig Position 4	PTP4	PTP5 [15:0]															
	0x 1 1A	Pos Trig Position 3	PTP3	PTP3 [15:0]															
	0x 1 19	Pos Trig Position 2	PTP2	PTP2 [15:0]															
	0x 1 18	Pos Trig Position 1	PTP1	PTP1 [15:0]															
	0x 1 17	PT Auto-Clear & Hysteresis	PTAH	PTAUTOCLR	HYSTERESIS [14:0]														
	0x 1 16	Position Trigger 8&7 Control	PTC87	PT8ACT [1:0]		PT8DIR [1:0]		PT8MAP [3:0]				PT7ACT [1:0]		PT7DIR [1:0]		PT7MAP [3:0]			
	0x 1 15	Position Trigger 6&5 Control	PTC65	PT6ACT [1:0]		PT6DIR [1:0]		PT6MAP [3:0]				PT5ACT [1:0]		PT5DIR [1:0]		PT5MAP [3:0]			
	0x 1 14	Position Trigger 4&3 Control	PTC43	PT4ACT [1:0]		PT4DIR [1:0]		PT4MAP [3:0]				PT3ACT [1:0]		PT3DIR [1:0]		PT3MAP [3:0]			
	0x 1 13	Position Trigger 2&1 Control	PTC21	PT2ACT [1:0]		PT2DIR [1:0]		PT2MAP [3:0]				PT1ACT [1:0]		PT1DIR [1:0]		PT1MAP [3:0]			
	0x 1 12	Sample Indicator Control	SIC									SAUTOCLR [1:0]		SCTRL [1:0]		SMAP [3:0]			
	0x 1 11	Sensor Type	STYPE									SUBTYPE [3:0]				TYPE [3:0]			
	0x 1 10	DAC Control Word	DACCW	DACNV [15:8]								DACEN	-	-	DACADDR [2:0]			DACOP [1:0]	
	0x 1 0F	DAC Limit Y	DACLIMY	DACLIMY[15:0]															
	0x 1 0E	DAC Limit X	DACLIMX	DACLIMX[15:0]															
	0x 1 0D	DAC Position D	DACPOSD	DACPOSD[15:0]															
	0x 1 0C	DAC Position C	DACPOSC	DACPOSC[15:0]															
	0x 1 0B	DAC Position B	DACPOSB	DACPOSB[15:0]															
	0x 1 0A	DAC Position A	DACPOSA	DACPOSA[15:0]															
	0x 1 09	LED Control Word	LEDCW	LEDTHRESHOLD [11:0]												LEDMAP [3:0]			
	0x 1 08	Sensor Constants	CONST	-	-	-	-	-	-	-	-	FCSEL [3:0]				ABSSEL [3:0]			
	0x 1 07	Result Register F	RESF	RESF [15:0]															
	0x 1 06	Result Register E	RESE	RESE [15:0]															
	0x 1 05	Result Register D	RESD	RESD [15:0]															
	0x 1 04	Result Register C	RESC	RESC [15:0]															
	0x 1 03	Result Register B	RESB	RESB [15:0]															
	0x 1 02	Result Register A	RESA	RESA [15:0]															
	0x 1 01	Pos Trig Enables/Flags	PTEF	PT8E	PT7E	PT6E	PT5E	PT4E	PT3E	PT2E	TPT1E	PT8F	PT7F	PT6F	PT5F	PT4F	PT3F	PT2F	PT1F
	0x 1 00	Sensor Control Word	SCW	SENSOR [3:0]				PIE	PIF	INCE	INCF	SIE	SIF	NEW	VALID		TRIG	CONT	GO
System	0x 0 0F	Device ID	SYSID	SYSID [15:0]															
	0x 0 0E	System Version Number	SYSVER	SYSVER [15:0]															
	0x 0 0D	Bootloader Version Number	BOOTVER	BLVER [15:0]															
	0x 0 0C	Save Key	SAVEKEY	SAVEKEY [15:0]															
	0x 0 0B	System Identity	CTUID	CTUID [15:0]															
	0x 0 0A	(Reserved)																	
	0x 0 09	(Reserved)																	
	0x 0 08	(Reserved)																	
	0x 0 07	(Reserved)																	
	0x 0 06	(Reserved)																	
	0x 0 05	(Reserved)																	
	0x 0 04	(Reserved)																	
	0x 0 03	System DAC Register	SYSDAC	DACCAL	-	-	-	-	-	CPOL	CPHA					DACFORMAT [2:0]			DACSON
	0x 0 02	IO Pin Types	SYSIO	-	-	-	-	INT6AH	INT6DO	INT5AH	INT5DO	INT4AH	INT4DO	INT3AH	INT3DO	INT2AH	INT2DO	INT1AH	INT1DO
	0x 0 01	Continuous Sample Interval	SYSI	SYSI [15:0]															
	0x 0 00	System Control Word	SYSCW	RESET	BOOTLOAD	SAVE	FACTORY												PWRDN

Read Only | Read / Write | Read / Write to 0

Figure 24 Register Map Detail

9.1 SYSCW: System Control Word

SYSCW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x000	RESET	BOOTLOAD	SAVE	FACTORY	-	-	-	-	-	-	-	-	-	-	-	PWRDN
Access	R/W	R/W	R/W-1	R/W-1	R	R	R	R	R	R	R	R	R	R	R	R/W

Factory default value = 0x0000

Writing a 1 to the RESET bit will result in a device reset at the end of the SPI transaction. Registers will return to their default values and measurements will be aborted.

Writing a 1 to the PWRDN bit pauses measurements in progress and puts the CAM312 chip into a low power state. To take the CAM312 chip out of this state and resume any measurements in progress, toggle nSS low. This operation may take the form of a dummy SPI read, whose results should be discarded.

Writing a 1 to the BOOTLOAD bit resets the CAM312 chip at the end of the SPI transaction. When the CAM312 chip comes out of reset, it will remain in Bootloader Mode (section 12) until the next reset.

Writing a 1 to the SAVE bit, together with 0x0C1C to the SAVEKEY register, will result in the current register contents being made the Configurable Defaults (section 0). Writing a 1 to the FACTORY bit, together with 0x0C1C to the SAVEKEY register, will result in restoration of the factory default register values. After the SAVE or FACTORY operations the CAM312 chip will reset.

9.2 SYSI: System Interval Register

SYSI	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x001	SYSI [15:0]															
Access	R/W															

Factory default value = 0x000A

The CAM312 includes an option for the CAM312 to take measurements continuously, without the host having to initiate each one over SPI. The SYSI register controls the time between the start of each sensor measurement. The time is the value of SYSI multiplied by 100µs, and is approximate.

If Sensor 1 and Sensor 2 are both configured for continuous operation, each measurement on sensor 1 is immediately followed by a measurement on sensor 2. SYSI controls the time between the start of each measurement on sensor 1.

Table 19 Example SYSI values

SYSI	Time between start of measurements	Comments
0	Each measurement immediately follows the previous one	For continuous measurement at fastest rate
5	500µs	Smallest practical value for regularly timed measurements on a single Type 4 sensor, or a Type 6 sensor with INCE=1
		Smallest practical value for regularly timed measurements on a Type 6 sensor with INCE=0
10	1000µs (1.0ms)	Smallest practical value for regularly timed measurements on two Type 4 sensors
100	10ms	100 per second
1000	100ms	10 per second
65535	6553.5ms (6.5 seconds)	Longest interval

9.3 SYSIO: System IO Configuration

SYSIO	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x002	-	-	-	-	INT 6AH	INT 6DO	INT 5AH	INT 5DO	INT 4AH	INT 4DO	INT 3AH	INT 3DO	INT 2AH	INT 2DO	INT 1AH	INT 1DO
Access	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Factory default value = 0x0000

The SYSIO register controls each IO pin's behaviour. Each pin may be configured for active low or active high with the coding of Table 30. Independently, each pin may be configured for open drain or digital with the coding of Table 31.

Table 20

INTnAH	Function
0	Active Low
1	Active High

Table 21

INTnDO	Function
0	Open Drain
1	Digital Output

9.4 CTUID: CTU Identity

CTUID	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00B	CTUID[15:0]															
Access	R															

Default value = 0x030C

This CTU Identity register may be used to read the identity of the connected CTU chip: 0x030C corresponds to the CAM312.

9.5 SAVEKEY: Save Key

SAVEKEY	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00C	SAVEKEY[15:0]															
Access	R/W															

Default value = 0x0001

This system register is used to prevent accidental changes being made to register defaults. For the SAVE and FACTORY operations to take effect, its value should be set to 0x0C1C immediately beforehand.

9.6 BOOTVER: Bootloader Version Number

BOOTVER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00D	Bootloader Version Number [15:0]															
Access	R															

Factory default value = 0x0202

The BOOTVER register contains the fixed revision number for the CAM312 chip's Bootloader Code, and is read-only.

9.7 SYSVER: System Version Number

SYSVER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00E	System Version Number [15:0]															
Access	R															

Factory default value = 0x0100 ("V1.0")

The SYSVER register contains the version number of the CAM312 chip's Application Code, and is read-only. It is updated when new code is successfully updated using the bootloader (section 12).

9.8 SYSID: System Device ID

SYSID	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00F	SYSID[15:0]															
Access	R/W															

Factory default value = 0xABCD

The System Device ID is a host-writeable word, and appears as the first word of every SPI transaction (see section 8.3). It is recommended that the host verifies this value against the expected one, to assist detection of communication errors.

The SYSID may be used to identify different SPI slave devices connected to the same host. Any value may be chosen; it is of no significance to the CAM312 chip. However it is strongly recommended to avoid 0x0000, 0xFFFF and any of the possible Status Codes (section 10.10), since these may also result from communication errors or bootloader operation.

The Device ID may be used to detect or verify that a CAM312 chip reset has occurred. The host should write a new SYSID value, and any subsequent reset will cause SYSID to return to its default value.

9.9 SCW: Sensor Control Word

SCW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xn00	SENSOR[3:0]				0	0	INCE	INCF	SIE	SIF	NEW	VALID	-	-	CONT	GO
Access	R				R	R	R/W	R	R/W	R/W0	R/W0	R	R	R/W	R/W	R/W

Factory default value = 0xn000

The registers described above relate to system functions. The Sensor Control Word, and the other registers described below, relate to sensors connected to the CAM312 chip. More than one sensor may be connected, depending on sensor type, and these registers are distinguished by bits 8 to 11 of the address. Two Type 4 sensors may be connected, and the addresses of their SCW registers are 0x100 and 0x200.

The host can start a measurement on a sensor by setting its GO bit to 1. If the host also sets the CONT bit to 1 the CAM312 chip will measure that sensor continuously. In this case, the sample interval between measurements active sensors is configured with SYSI, see section 9.2. If a sensor's CONT bit is set to 0, setting its GO bit to 1 will result in a single measurement. The CAM312 chip will clear GO to 0 upon completion.

The VALID bit indicates that the last measurement result for the sensor was valid. The CAM312 sets the VALID flag when it determines the channel's target to be in range. The meaning of in range depends on the sensor and target, but typically means that it is physically aligned within specification and its resonant frequency is within specified limits.

The NEW flag indicates that new measurement data is available for the sensor. The CAM312 chip sets NEW to 1 when a measurement is completed. It is recommended that the host clears NEW back to 0 when reading result registers, using a multiple register write/read SPI transaction spanning SCW and the relevant results registers. That way, the host can unambiguously verify that the results it has collected from the CAM312 chip are new.

The SIF bit is the sample indicator flag, and SIE is the sample indicator enable bit. Sample indicators can be configured to activate an IO when a new, or a new valid, sensor measurement is available. When sample indicators are suitably configured (see section 9.12), the SIE bit controls whether sample indicators are enabled. Once activated, the host may clear a sample interrupt by writing a 0 to SIF (see also section 11.4 concerning timing).

INCE and INCF are for sensor Types 2 and 6, which support Incremental Mode. The INCE bit controls whether Incremental Mode is allowed. The INCF bit is a flag that indicates when an incremental measurement was actually performed. See section 10.7 for details.

SENSOR[3:0] equals the sensor number. The host may check that SENSOR equals the requested sensor number, to ensure that measurement results are associated with the expected sensor.

9.10 RESA...RESF: Results Registers

RESA … RESF	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xn02 … 0xn07	RESA [15:0] … RESF [15:0]															
Access	R															

Factory default values = 0x0000

A sensor's results registers contain the results of the last measurement to complete on that sensor. The CAM312 chip supports different sensor types. The interpretation of result registers depends on the sensor type as described in Table 22.

Table 22 Interpretation of measurement results

Register	Sensor Type	
	4	**2 and 6**
RESA	CtuReportedPositionI16	CtuReportedPositionI32 high word
RESB	AmplitudeU16	CtuReportedPositionI32 low word
RESC	RelativeFrequencyI16	AmplitudeAU16
RESD	Not used	AmplitudeBU16
RESE	Not used	RelativeFrequencyI16
RESF	Not used	BAPositionMismatchI16

CtuReportedPosition may be converted into measurement units with Equation 4 below. Sin Length is a characteristic of the sensor, and is quoted in sensor datasheets. Type 2 and 6 sensors have fine and coarse pitches. Sin Length should be set to Fine Pitch for use in Equation 4.

Equation 4 Interpreting position result

$$ReportedPosition = \frac{CtuReportedPosition}{65536} \times SinLength$$

Reported Position is a signed quantity which is nominally 0 when the Target Origin is aligned with the Sensor Origin. This is usually at the centre point of the sensor's travel.

CtuReportedPosition will be forced to 0 following an invalid measurement when the target is out of range. The host can use the VALID bit of the SCW register to distinguish this condition from zero Reported Position.

Amplitude is a measure of inductive signal strength and influences system performance, particularly resolution. Type 2 and 6 sensors have two Amplitude results, one based on readings from fine sensor coils (AmplitudeA) and one for coarse coils (AmplitudeB). The coarse value is usually significantly less than the fine. References to Amplitude in a sensor's datasheet are to Amplitude A unless otherwise noted.

Relative Frequency is the CAM312 chip's approximate measurement of the frequency difference in Hz between the target and the CAM312 chip's Centre Frequency, whose nominal value is specified in Table 15.

BA Position Mismatch is specific to Type 2 and 6 sensors. It is scaled in the same way as Reported Position using Equation 4. When results are from Incremental Mode operation (INCF=1), BA Position Mismatch is the difference between the current and previous reported position. In absolute mode (INCF=0), BA Position Mismatch is the difference between position readings from the fine and coarse sensor tracks. In each of these cases BA Position Mismatch is an indication of system health. Small values are healthy, while values close to SinLength/2 indicate potential for error in position measurement caused by skipping a fine period (section 10.7).

9.11 STYPE: Sensor Type Register

STYPE	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xn11	-	-	-	-	-	-	-	-	SUBTYPE[3:0]				TYPE[3:0]			
Access	R	R	R	R	R	R	R	R	R/W (all sensors)				R/W (sensor1 only)			

Factory default value = 0x0004

The CAM312 chip is designed to operate with different types of sensor, see Table 1. To operate different sensor Types, the host must write the appropriate number to sensor 1's TYPE field before any position measurements. Other sensors' TYPE fields are read only. They will read either 0 if measurement on this sensor is not allowed or sensor 1's TYPE if measurement is allowed.
Some sensors have Subtypes. For example "Type 6.5" is Type 6, Subtype 5. For each sensor used, the SUBTYPE bits should be set to the sensor's Subtype.

Table 23 lists example sensors of sensor configurations, and the settings required for each STYPE register.

Table 23 STYPE settings required for example configurations

Connected sensors	STYPE sensor 1	STYPE Sensor 2
One Type 4 sensor connected to sensor 1 (COS1, SIN1)	0x0004	Don't care
One Type 4 sensor connected to sensor 2 (COS2, SIN2)	0x0004	0x0004
Two Type 4 sensors	0x0004	0x0004
Type 6.5 sensor (Type 6, Subtype 5)	0x0056	Don't care
Type 2.12 sensor (Type 2, Subtype 12)	0x00C2	Don't care

9.12 SIC: Sample Indicator Control Register

SIC	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xn12	-	-	-	-	-	-	-	-	SAUTOCLR[1:0]		SCTRL[1:0]		SMAP[3:0]			
Access	R	R	R	R	R	R	R	R	R/W		R/W		R/W			

Factory default value = 0x0000

Sample indicators signal whether the CAM312 has new, or new valid, measurement results available for a sensor. The function is configured with SCTRL[1:0], see Table 24.

Table 24 SCTRL function

SCTRL[1:0]	Function
0	No sample indicators
1	Set on any new position
2	Set if VALID flag set
3	Reserved

Sample indicators can be configured to control the CAM312 chip's digital IOs. SMAP[3:0] configures which of the available IOs is used for the sensor's sample indicator. See Table 25 for how this bit field is encoded.

Table 25 SMAP function

SMAP[3:0]	IO pin mapping
0	Not mapped to an IO
1	IO1
2	IO2
3	IO3
4	IO4
5	IO5
6	IO6
7-15	reserved

Sample indicators can be reset by the host over the SPI interface by writing a 0 to the sample indicator flag SIF, see section 9.9. Alternatively, they may be "auto-cleared". SAUTOCLR[1:0] controls sample indicator auto-clear behaviour. Table 26defines how this bit field is encoded.

Table 26 SAUTOCLR function

SAUTOCLR[1:0]	Auto clear behaviour
0	Autoclear OFF
1	Clear during measurement
2	Clear after measurement
3	Reserved

Sample indicators can be used to generate an IO whose state reflects whether the sensor's last measurement was VALID or not. Set SCTRL to 2 ("on valid") and SAUTOCLR to 2 ("after measurement"). The IO will only change state if there is a change in VALID.

Sample indicators can be used to create an active edge on an IO each time a measurement has completed…

- If each measurement is initiated by the host over SPI by setting GO=1, then the host can clear SIF during that same transaction. In this case the IO will clear after the SPI transaction (subject to timing parameter TnSSH2IOch of Table 17). In this case use SAUTOCLR=0 (factory default value).
- If two sensors are mapped to the same IO then configure each sensor to "clear during measurement" (SAUTOCLR=1).
- If sensors are sampling continuously (CONT=GO=1) then configure each such sensor to "clear during measurement" (SAUTOCLR=1). See section 10.6.

10 System Operation

10.1 Reset, Validity Check and Reading Versions

The CAM312 CTU chip is internally reset following power on, when nRESET is toggled or when the host writes a 1 to the RESET bit in the SYSCW register (section 9.1).

Following a reset, the CAM312 performs internal validity checks, as illustrated in the flowchart of Figure 25.

Validity checks include a checksum of the CAM312 chip's FLASH memory contents, including Application Code. The time taken for these checks is TVALIDCHECK, as specified in Table 17. For normal operation, the host should allow at least TVALIDCHECK(MAX) between a reset and the first SPI communication with the CAM312, to avoid interrupting the validity checks.

The CAM312 has a set of 4 registers that contain version numbers, from CTUID (address 0x000B, see section 9.4) to SYSVER (0x000E, section 9.8). It is recommended that the host reads these 4 registers as the first SPI transaction after any reset. If validity checks passed successfully, the CAM312 will return the SYSID register contents (factory default 0xABCD) as the first word, followed by the version numbers.

If the CAM312 did not pass its validity checks it will return 0x10AD as the first word. This will usually be because Application Code is absent. Please refer to section 12 for details of loading code using the CAM312 chip's bootloader.

The CAM312 chip will also return 0x10AD as the first word if validity checks were interrupted by an SPI transaction before they completed.

Once the CAM312 chip has completed its validity checks and the host has optionally read out version numbers, the host can configure the CAM312 chip for taking measurements.

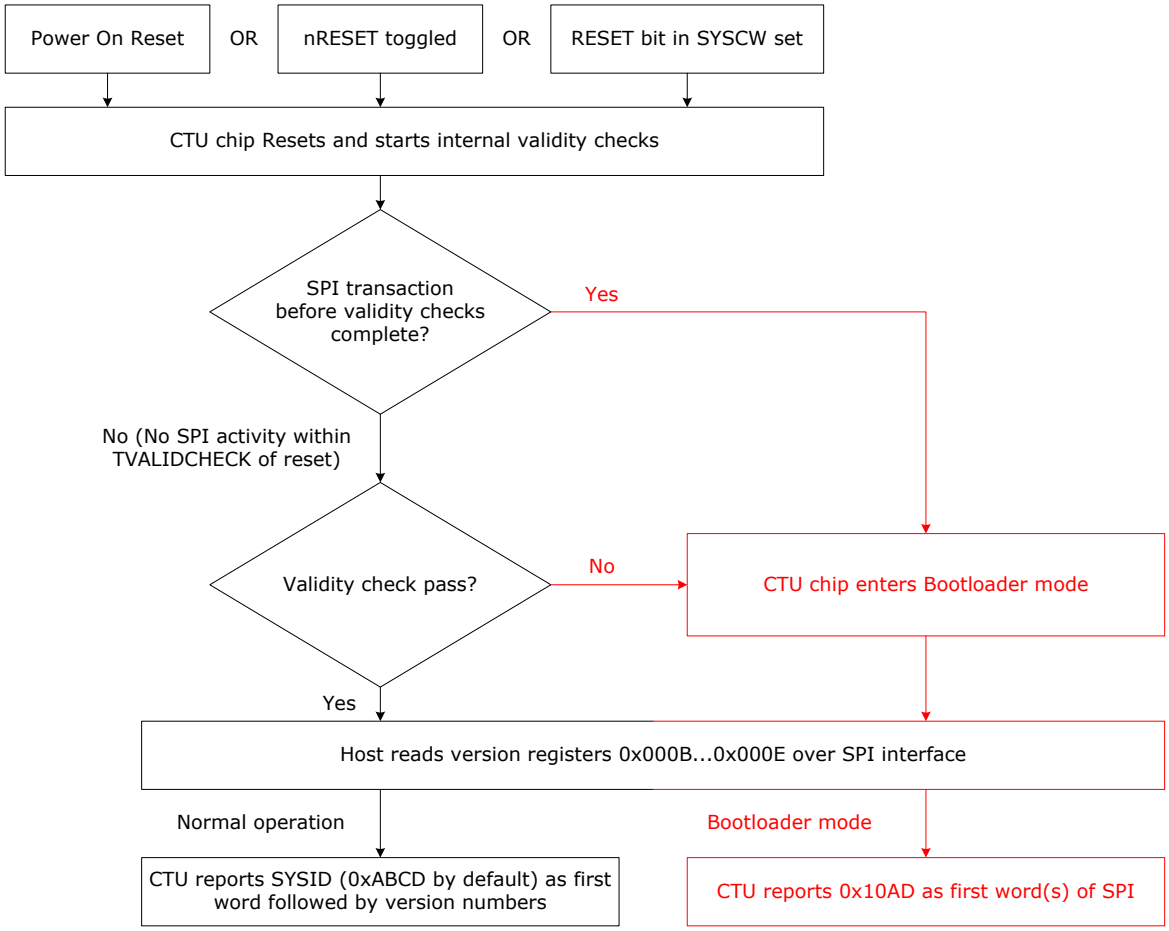

Figure 25 CAM312 reset and validity checking process

10.2 Configuration

Before taking measurements, the host must configure the CAM312. This is done by writing appropriate register contents to registers used to configure the required functions. Table 27 lists registers used for configuration, when they are needed, a summary of their function and where to find a detailed description.

Table 27 Registers to configure before measurement

Registers	When to use	Description	See...
SYSID	Optional	The host may change the SYSID value from its default value following a reset. This can help distinguish different CAM312 chips connected to the same SPI bus. It can also be used to detect an unexpected CAM312 reset.	Section 9.8
STYPE sensor 1	Essential	Tells CAM312 what type of sensor is connected to either or both sensor 1 and sensor 2	Section 9.11
STYPE sensor 2	If sensor 2 connected	Tells CAM312 what type of sensor is connected to sensor 2, if used	
SYSIO	If IOs used	Configures each IO for open drain or digital, and active high or active low	Section 9.3
SIC sensor 1	If sensor 1 sample indicator required	Tells CAM312 which IO to use for sensor 1 sample indicator, when to set and when to clear	Section 9.12
SIC sensor 2	If sensor 2 connected and sample indicator required	Tells CAM312 which IO to use for sensor 2 sample indicator, when to set and when to clear	
SYSI	Optional	Time between measurements operating in continuous mode (CONT=1)	Section 9.2

It is recommended to use write read single register SPI to access each register, as described in Figure 17. After each SPI transaction, the nSS SPI line must remain high for long enough for the CAM312 to complete each configuration step. The minimum high time is parameter TnSSHR2nSSLR(min) which is specified in Table 17.

Configuration registers may be accessed in any order.

SPI write read access returns the previous register settings, as they were before the SPI transaction. To check the new register settings are in place, the host may perform SPI read transactions.

10.3 Repeated Single Shot Measurement, One Sensor

In most applications the host needs regular measurement results from the CAM312. The simplest mode of operation is to repeat a single SPI transaction, which both starts a measurement (GO=1) and reads the results of the previous measurement. This process is illustrated in Figure 26.

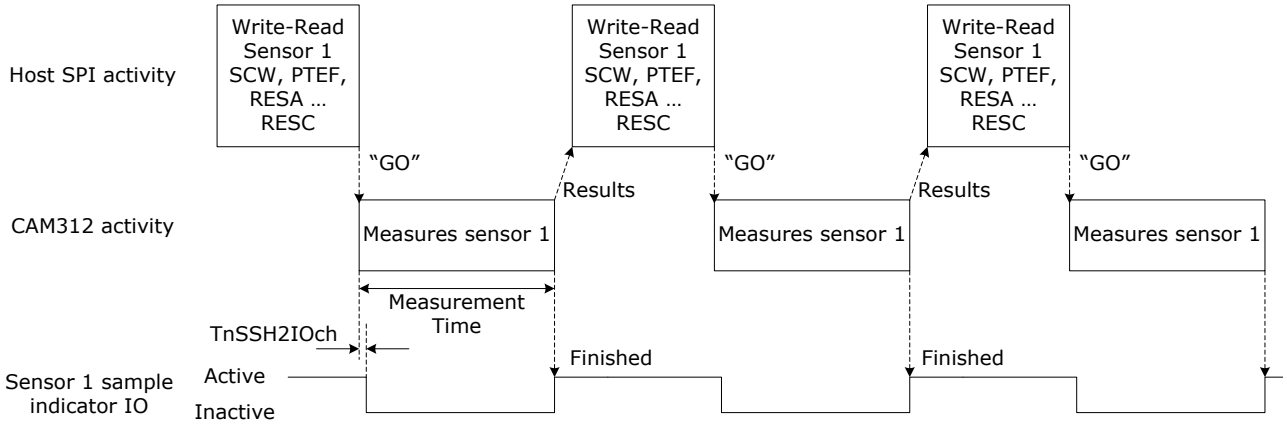

Figure 26 Repeated Single Shot Measurement, One Sensor

The host should use a multiple register access SPI transaction as illustrated in Figure 18. The first register to access is the sensor's SCW. If there is one Type 2 or 6 sensor connected, only sensor 1's SCW register may be accessed. If there are two Type 4 sensors connected, the host may access either sensor 1 or sensor 2's SCW register, to perform measurements on sensor 1 or sensor 2. To alternate measurements between two sensors please refer to section 10.4 below.

The SCW register includes the GO bit which must be set to 1 each time so that the CAM312 performs another measurement. The CONT bit must be 0, so that CAM312 measurements are only initiated by the host and do not happen asynchronously. It is recommended to clear the NEW bit to 0, so that the host can identify whether the next measurement results are really new ones. The SIE bit must be set if the sensor's sample indicator is required. The SIF bit must be cleared to 0 so that the sample indicator returns to its inactive state following the SPI transaction ready for the next measurement. For Type 2 or Type 6 sensors, the INCE bit may be set to allow incremental mode , see section 10.7. The location of each bit within the SCW register is shown in section 9.9.

The number of words in the SPI transaction depends on how many results are needed. It is strongly recommended to read all results registers for the sensor Type in use (section 9.10). For example, if the sensor is Type 4, the SPI transaction should span SCW, PTEF, RESA, RESB and RESC. The PTEF and results registers are all read only, so it does not matter what data the host sends over the SPI MOSI line following the SCW register. 0x0000 is recommended for simplicity.

Once the SPI transaction has ended, the CAM312 starts a measurement, and clears any sample indicator IO mapped to the sensor. The time taken to clear the sample indicator is TnSSH2IOch, whose maximum value is specified in Table 17.

New measurement results are available for the host to read once the measurement has completed. The maximum time required for the measurement depends on sensor Type and operating mode. This Measurement Time is measured from the end of the SPI transaction setting GO to when measurements are available, as shown in Figure 26. Values are specified in Table 28. If used, a sample indicator IO will activate when new measurements are available. If not, the host should wait for at least the Maximum Measurement Time before performing another SPI transaction.

The host may then perform another SPI transaction to set GO again for the next measurement, and to read the results of the measurement just completed. These measurement results are found in the SCW register and in the results registers.

The SCW register includes the VALID bit, which indicates whether or not the measurement was VALID. It is important for the host to read the VALID bit, because results registers only contain valid data when VALID is set. It may take a number of measurements before the VALID bit is set, when the target is in range, see section 7.

The CAM312 chip sets the NEW bit each time a sensor's measurement completes. If the host reads NEW=0 then this indicates that there has been no new measurement since the previous SPI transaction, when NEW was cleared to 0. This could be caused by allowing insufficient time for the measurement to complete.

For sensor types which allow incremental mode, INCF indicates whether the measurement was actually an incremental one (1) or whether it was actually absolute (0), see section 10.7.

If valid, results registers may be interpreted according to section 9.10.

10.4 Repeated Single Shot Measurement, Two Sensors

The CAM312 chip can measure two Type 4 sensors. The host may take alternating measurements from two sensors with the process illustrated in Figure 27. Once a measurement has completed on sensor 1, the host may perform an SPI transaction reading sensor 2 results and setting sensor 2 to GO again. Once a measurement has completed on sensor 2, the host may perform an SPI transaction reading sensor 1 results and setting sensor 1 to GO again.

Please refer to section 10.3 for details of the SPI transactions required. The only difference between the two sensors is the address of the SCW register.

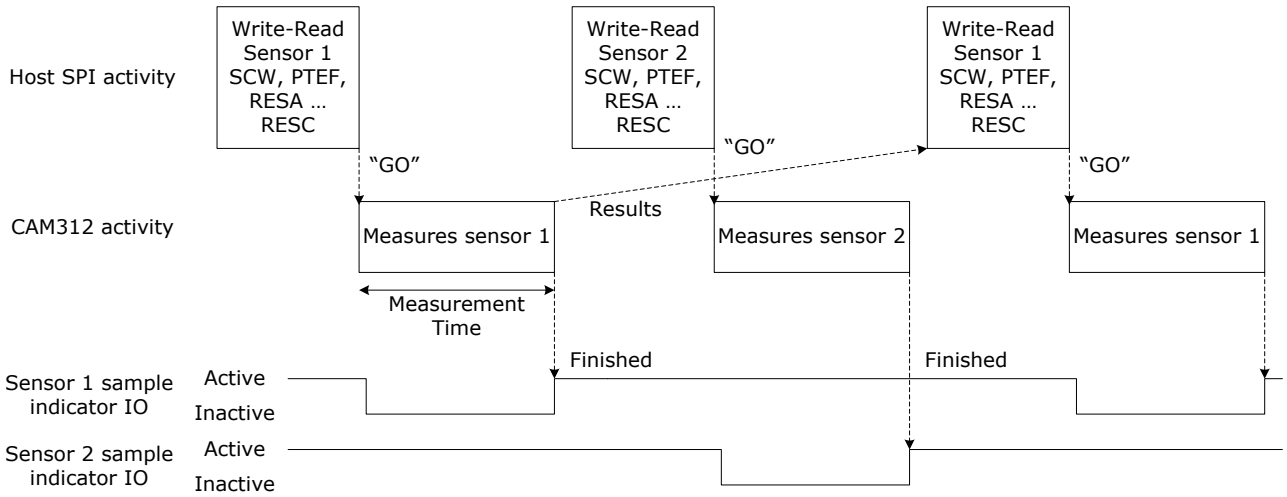

Figure 27 Repeated Single Shot Measurement, two sensors

Figure 27 illustrates two sample indicators, one for each sensor. The host can respond to the activation of sensor 1's sample indicator with a sensor 2 SPI, and the activation of sensor 2's sample indicator with a sensor 1 SPI.

Another option is to map both sensor sample indicators to the same IO, illustrated in Figure 28. Each time the IO activates the host can perform the next SPI transaction. In this case the SAUTOCLR bits of the SIC register must be set to "clear during measurement" as detailed in section 9.12, because clearing SIF only clears each sensor's sample indicator and not the other's. Note that the active to inactive IO edge no longer coincides with the end of each SPI transaction.

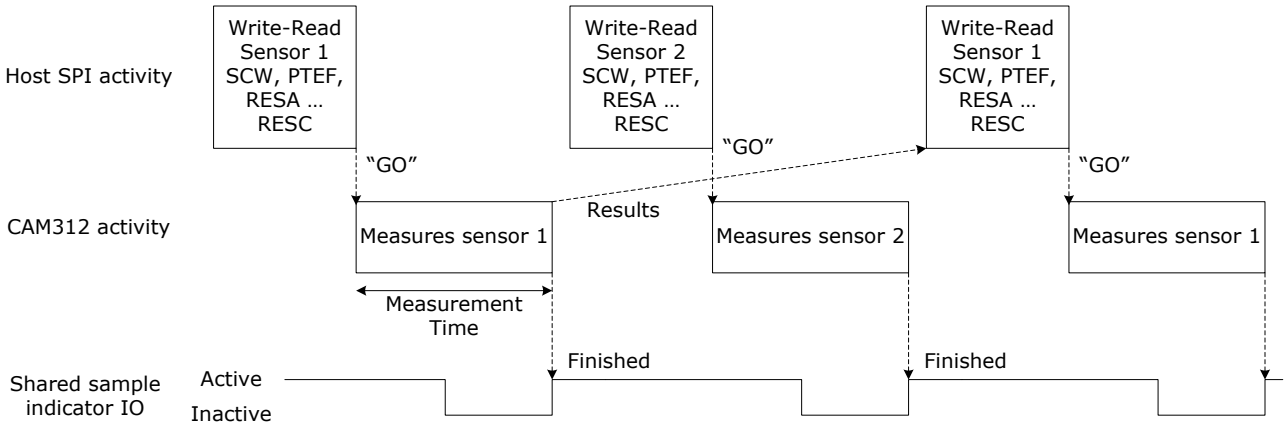

Figure 28 Repeated Single Shot Measurement, two sensors sharing a sample indictor IO

10.5 Isolated Single Shot Measurement

The measurement processes of sections 10.3 and 10.4 only require one SPI transaction per measurement. Each SPI transaction starts a measurement on a sensor, and reads back the measurement results from the preceding measurement on that sensor. If the host only requires occasional measurements, or measurements are taken at a low sample rate, there can be a long time interval between the CAM312 completing a measurement and the host reading the results.

This interval can be eliminated by performing two SPI transactions for each measurement: one to kick off the measurement and another to read results when they are ready. This process is illustrated in Figure 29.

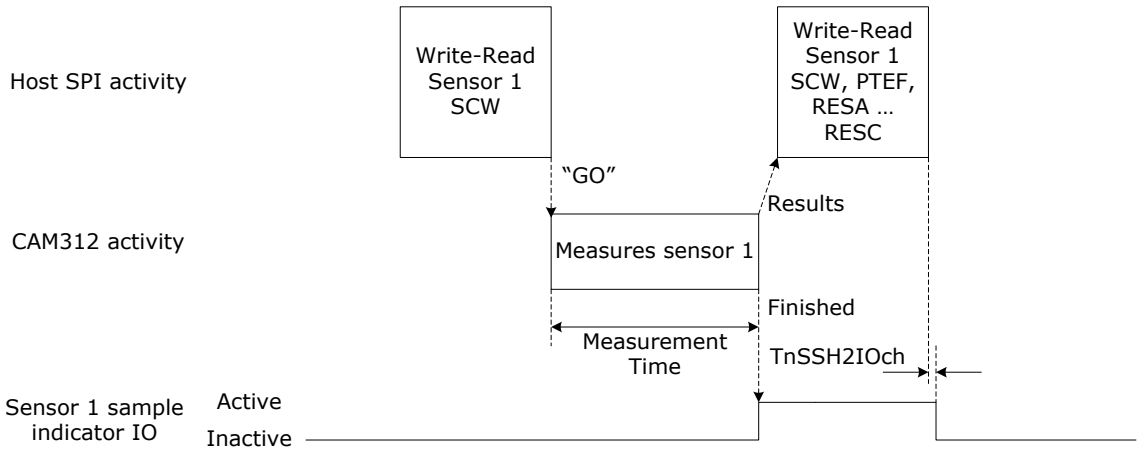

Figure 29 Isolated Single Shot Measurement

The SCW register contents used to initiate the measurement should be set up in the same way described in 10.3, including GO=1, CONT=0, NEW=0, SIE and INCE.

The SPI transaction used to read results should span SCW, PTEF and the results registers as before. It should be a write read transaction with the SCW register's GO=0, CONT=0 and NEW=0.

The host interprets results in the same way, including SCW register's VALID bit and the results registers themselves.

If two Type 4 sensors are connected, the process for an isolated single shot measurement can be applied to both sensors, one after the other.

10.6 Continuous Measurement

Continuous Measurement is for applications where the CAM312 must take repeated measurements on its own, without the host initiating each measurement. A typical application is where the CAM312 is connected to an external DAC and the CAM312 updates the DAC's output each measurement. This is described in section 11.

The host configures the CAM312 for continuous operation in the same way as single shot measurements, as summarised in section 10.2. The host must write a suitable value to the SYSI register to control the Continuous Interval between measurements, see section 9.2.

Next, the host must write to each sensor's SCW register, including GO=CONT=1. If the sensor is Type 2 or Type 6, the host must write an appropriate value for the INCE bit, to either allow or disallow incremental mode. It is recommended to use absolute measurements (INCE=0) to guarantee no loss of absolute position, unless the system needs the fastest possible sample rate and there is no risk of a Fine Skipping Error (section 10.7).

Where only a single sensor is configured for continuous operation, the CAM312 will sample continuously, with an internal timer starting each measurement. If the sensor's sample indicator is mapped to an IO and configured to activate on each new sample and to auto-clear during each measurement (section 9.12), then it will activate as illustrated in Figure 30.

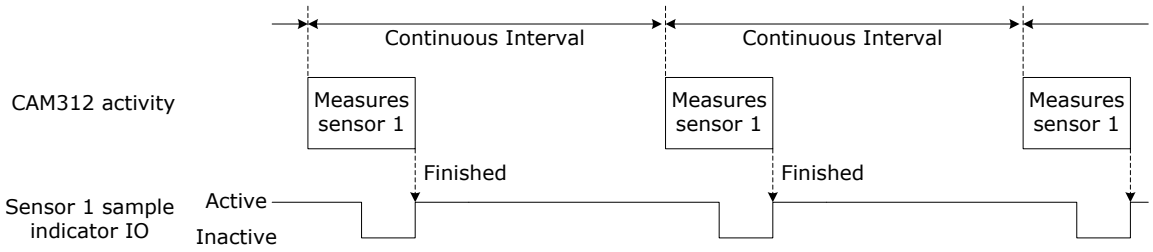

Figure 30 Continuous Measurement, Sensor 1

Where more than one sensor is configured for continuous operation, the CAM312 will measure the sensors in turn, one straight after the other, in order of sensor number. Continuous Interval is measured between successive starts of measurements on the lowest numbered sensor, as illustrated in Figure 31.

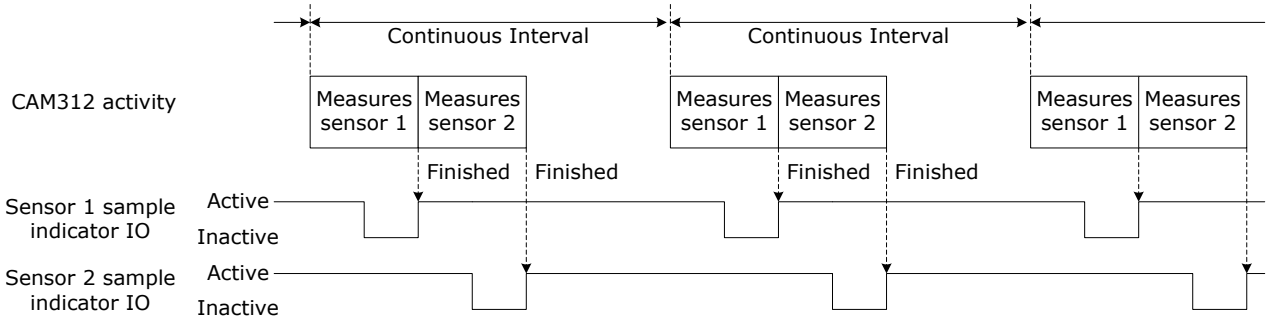

Figure 31 Continuous Measurement, Sensor 1 and Sensor 2

Figure 30 and Figure 31 show how the states of sample indicators change when configured to activate on each new sample (SCTRL=1) and to auto-clear during each measurement (SAUTOCLR=1). To obtain an IO whose state instead reflects whether or not a sensor's latest measurement was VALID, the host should configure sample indicators to activate only when its sensor is VALID (SCTRL=2), and to clear after each measurement (SAUTOCLR=2) if it is not (section 9.12).

The CAM312 can be configured to start continuous measurements after power is applied, without the CAM312 being connected to an SPI interface at the time. This is done using configurable defaults, as detailed in section 0. Register settings are the same as described above. However they are stored in the CAM312 chip's non-volatile memory as configurable defaults. This allows a CAM312 chip to operate autonomously without an SPI connection. A typical application is a product including the CAM312 chip to take measurements connected to a DAC to provide a digital output, as in section .

Although not normally recommended, it is possible for a host to read measurement results over SPI during continuous operation. Since the SPI and measurement timings may be asynchronous, the "Measurement in progress" SPI timings of Table 17 must be used.

10.7 Incremental Operation

Type 2 and 6 sensors have two pairs of sensor coils, coarse and fine. Both are patterned for sinusoidal sensitivity. Coarse coils deliver an absolute measurement of position, coarse position, and have relatively poor accuracy and resolution. This is represented by the wobbly upper graph of Figure 32. Fine coils deliver precise fine position, but are only incremental, represented by the middle graph. The CAM312 chip combines the two position measurements so that the position measurements that it reports to the host are always both precise and absolute, as illustrated in the lower graph.

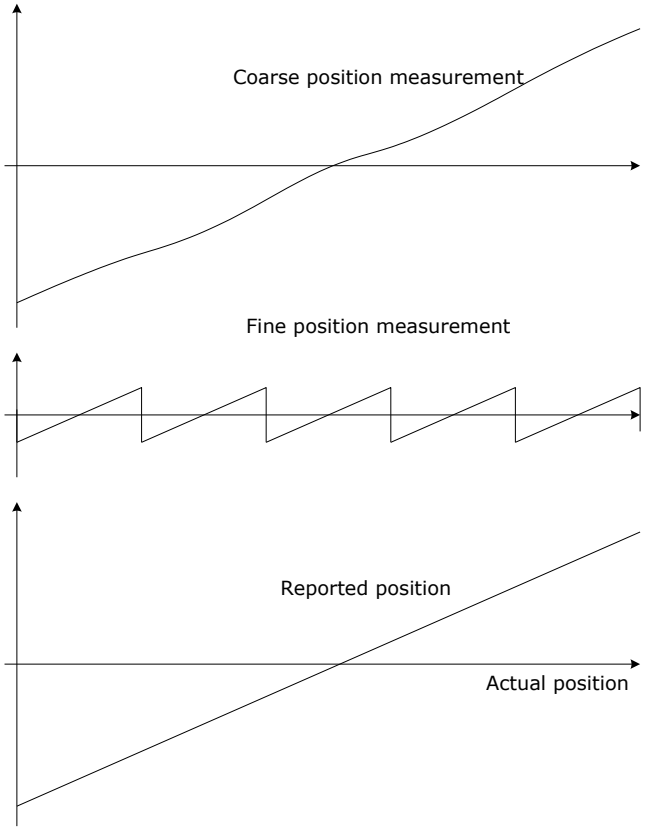

Figure 32 Combining coarse and fine measurements

When measuring such sensors, the CAM312 chip has two modes of operation: Absolute and Incremental. In Absolute mode, each CAM312 measurement includes measurements from both the fine and coarse coils. In Incremental mode, the CAM312 chip uses measurements from fine coils alone. It still reports absolute position, but does so by counting incremental periods from the last absolute measurement. Incremental measurements are only possible after a VALID absolute measurement. If the result of any measurement is NOT VALID, then the system will revert to Absolute mode until VALID once again.

When taking single shot measurements, the host may request Incremental mode measurements by setting the INCE bit (Incremental Enable) to 1. INCE is in the sensor's SCW register, which also contains the INCF bit (Incremental Flag). INCF indicates whether the current result registers contain data from an incremental (INCF=1) or Absolute (INCF=1) measurement.

For lowest supply current and the best available update rate the system should normally be operated in Incremental mode (INCE=1). However in this mode a fine period skipping error may occur if the target moves more than half a fine period per fine measurement. For a Type 6.3 sensor having SinLengthA=120°, the limit is 60°. When operating with a sample interval of 500µs, this means a rotation speed of 16000rpm, allowing for 20% safety margin. For this reason, and as a periodic integrity check, it is recommended to perform an occasional Absolute mode measurement (INCE=0) that will correct any such error. The host may choose when to perform the Absolute mode measurement, for example every 1000 samples or once any time the target's velocity is near zero.

It is strongly recommended to operate in Absolute mode with INCE=0 for operation with an external DAC. There is no chance for a host to request an occasional Absolute measurement, because there is no host connected.

10.8 Measurement Timings

Measurement Time is the time between the host requesting a measurement over SPI and its results being available for reading over SPI. It is measured from the rising edge of the nSS signal of the SPI transaction setting a sensor's GO bit and the activation of an associated sample indicator. Please see Figure 26.

Measurement Time depends on the Type of sensor connected and whether or not a measurement is VALID. For Type 2 and 6 sensors, the host also has the option to request incremental operation, by setting INCE=0. If the CAM312 is able to perform an incremental measurement it sets INCF, resulting in a shorter Measurement Time.

If VALID, measurement time also depends on the frequency of the resonator inside the target. The maximum measurement time is obtained when resonator frequency is at its lowest limit. This is when the reported Relative Frequency is approximately -25000Hz.

Table 28 specifies the Maximum Measurement Time as a function of Sensor Type, VALID and INCF. If the host performs an SPI transaction during a measurement the Measurement Time will increase and may exceed the value of Table 28.

Sample Interval is the time between successive measurements. When operating in repeated single shot mode, it is the time between successive SPI transactions used to start and read measurement results, as illustrated in Figure 33.

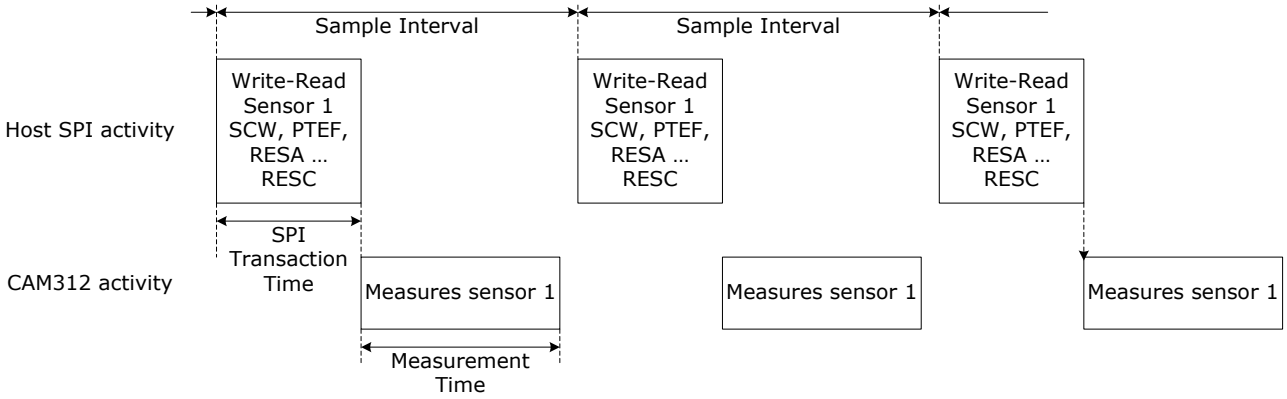

Figure 33 Definition of Sample Interval

Achievable Minimum SPI Transaction Times are detailed in section 8.7. In Table 28, the Minimum Sample Interval is these figures plus the Measurement Time. Maximum Sample Rate is the reciprocal of Minimum Sample Interval.

Group Delay is defined as the time between the effective "capture" point of position and the activation of a sample indicator at the end of measurement. Smaller values are obtained with Type 4 sensors, or Type 2 or 6 operating in Incremental Mode (INCF=1). Values are also listed in Table 28. Other sources of delay include the time it takes a host to respond to the sample indicator, and to

Table 28 Measurement Time and Group Delay

Sensor Type	VALID	INCF	Maximum Measurement Time	Minimum Sample Interval	Maximum Sample Rate	Group Delay
4	0	N/A	415µs	429µs	2300Hz	-
	1	N/A				200µs
2 or 6	0	N/A	640µs	660µs	1500Hz	-
	1	0				340µs
	1	1	425µs	445µs	2200Hz	200µs

10.9 Configurable Defaults

The CAM312 chip's default register contents can be configured over the SPI interface ("Configurable Defaults"). To change to new Configurable Defaults, the host should first write the required settings to the CAM312 chip's registers. The host should then write 0x0C1C to the SAVEKEY register (section 9.5) followed by a 1 to the SAVE bit (section 9.1). The CAM312 will then reset itself. After this reset, and each subsequent one, the CAM312 operation is determined by the saved Configurable Defaults.

The CAM312 chip's Factory Defaults can be restored by writing 0x0C1C to the SAVEKEY register followed by a 1 to the FACTORY bit (section 9.1). The CAM312 will reset itself following this operation.

The Configurable Defaults are stored in FLASH memory. The number of FLASH updates are limited (section 2.5), so updates to Configurable Defaults should be rare. The SAVE and FACTORY operations each count as one FLASH update. For most applications the update will be done only once when a product containing the CAM312 is manufactured.

The most common application for Configurable Defaults is to generate an analog output whose value depends on position. In this case there is no host SPI interface connection during normal operation. An SPI interface is connected temporarily during manufacturing of the customer's product, to program the Configurable Defaults. Configurable Default values will include operation in continuous mode (section 10.6), and settings required for the CAM312 to drive an external DAC (section 11).

It is strongly recommended NOT to use Configurable Defaults to store the configuration settings described in section 10.2, when measurements are to be read by a host over SPI. It is recommended to store the configuration settings within the host, and to write them afresh to the CAM312 after any reset. This avoids any possible discrepancy between what the host "thinks" the configuration settings should be and what is already preprogrammed into the CAM312. This discrepancy could in principle be avoided by the host reading all of the CAM312's register settings after a reset. However if the host were programmed to read and check settings, it might as well program them afresh instead. The exception is the SYSID register in cases when there are multiple CAM312 devices sharing the same SPI bus. In this case each device may have its own unique SYSID value, so that the host can check any data it receives comes from the expected device. The SYSID values would be programmed during manufacturing of the customer's product. Please refer to section 9.8 for more on the SYSID register.

Configurable Defaults revert to factory settings after an update of CAM312 Application Code (section 12). If it is important that custom settings survive an update, they should be read out of the CTU before the update process and written back and saved afterwards.

10.10 Status Codes

In normal operation the first word of each SPI transaction begins with the CAM312 chip's System ID, SYSID (section 9.8). Other codes may be encountered instead, and their meanings are described in Table 29.

Table 29 Status Codes

First word of SPI transaction	Status description
SYSID (0xABCD by default)	Normal operation
0x10AD	CAM312 chip is in Bootloader mode expecting Application Code over the SPI interface
0x0BAD	CAM312 chip is in Bootloader mode and has detected SPI transactions that do not include valid Application Code
0x600D	Bootloader data block transfer has been successful
Words starting 0xE	Reserved

If Status Codes relating to Bootloader mode are seen unexpectedly, they are usually due to SPI interface activity too soon after a reset (section 10.1). If they do not appear to be related to an intended reset, it is likely that an unintended reset occurred, for example due to an unstable power supply voltage or unexpected activity on the CAM312 chip's nRESET pin.

10.11 Supply Current

Table 30 illustrates typical current consumption figures for the system. These are measured from the VSUPPLY line, which supplies both the CAM312 chip and the excitation circuitry. It is therefore the total of all current needed to supply the sensor system.

Current consumption depends on sample rate. For Type 2 and 6 sensors, it also depends on whether the CAM312 is operating in incremental or absolute modes (section 10.7).

Table 30 includes both average and peak current values. Peak current occurs while excitation waveform is being generated (Figure 5) to drive current into the excitation coil.

Table 30 Typical current drawn from VSUPPLY

Sensor	Samples / Second	Average Current	Peak Current (C_EXSUP=10µF)	Peak Current (C_EXSUP=100µF)
Type 4 (100mm Type 1 Linear Sensor)	2000	35mA	80mA	45mA
Type 2 (350mm Type 2.12 Linear Sensor)	1000 (INCE=0)	38mA	100mA	60mA
	2000 (INCE=1)	38mA		
Type 6 (35mm Type 6.3 Rotary Sensor)	1000 (INCE=0)	35mA	80mA	45mA
	2000 (INCE=1)	35mA		

Peak current depends on the value of the excitation decoupling capacitor C_EXSUP. The minimum recommended value is 10µF, as specified in sections 3.3, 4.2 and 5.2. A higher value may be used. Table 30 includes peak current values for both 10µF and 100µF to illustrate the difference.

If an application only requires a relatively low sample rate, for example 100 samples per second, the peak current may be reduced further by increasing the value of R_EX. The value should be chosen so that the peak voltage drop across R_EX is no more than 0.3V.

Care must be taken to ensure the VSUPPLY line's voltage remains above the minimum Operating Supply Voltage specified in Table 3 at all times, including when peak current is being drawn.

11 Analog Output from an External DAC

This is a planned feature for the CAM312 chip. Please refer to the CAM204 datasheet for details.

12 Bootloader Operation

12.1 Overview

The CAM312 chip's internal software is partitioned into two fields: Application Code and Bootloader Code. The Application Code is responsible for normal CAM312 chip operation including measurements, with communication through the register interface described in section 10. The Bootloader Code can be used to update the Application Code using the CAM312 chip's SPI interface. In normal operation, the version number of the Application Code (the System Version Number) can be read over the SPI interface from the SYSVER register (section 9.7). The version number of the Bootloader Code can be read from the BOOTVER register (section 9.6).

The procedure for uploading new Application Code over the CTU chip's SPI interface is specified in this section. These details will be required if the host processor is required to perform the update process. The upload procedure may alternatively be performed by a PC communicating with the CAM312 chip over the SPI interface using CambridgeIC's CTU Adapter.

12.2 Applications

New versions of Application Code are typically released to enable new features. For example the planned addition of DAC output (section 11) and support for new Sensor Types. Instead of buying a new stock of chips, a customer can program existing chips with the new code.

12.3 CTU Firmware File Format

New CAM312 Application Code is provided in the CTU Firmware File format (.cff). This comprises a Header Block, a Data Block and a Checksum Word. The Header Block is plain text (each byte representing a text character using ASCII codes), while the Data Block and Checksum Word are binary.

The Header Block can be viewed on a PC as a text file, for example using *WordPad* or dedicated hex and binary code editing software such as *Hex Editor Neo*. The text includes version number, build date and a description of the CRC algorithm that can be used to checksum the Data Block.

The Header Block comprises rows that start with the "#" character and end in carriage return line feed ("<CR><LF>"). The data block can be identified by searching for the character after <CR><LF> that is not "#". In byte representation, this means the first byte after the pair of bytes 0x0D, 0x0A which is not 0x23.

The Data Block comprises the remaining bytes in the .cff file. It always incudes an even number of bytes, so that it includes an integer number of words. The last two bytes are the Checksum Word for the Data Block. The Checksum Word may be used to verify that the Data Block is valid and uncorrupted.

12.4 Bootloader Process

The Bootloader works with the process illustrated in Figure 36. The first step is to identify whether or not the CAM312 chip already has valid Application Code, because this determines which Bootloader entry method to use.

If the CAM312 does include Application Code already, or unsure, the host must use the "BOOTLOAD Bit Entry Method". The host must first set the BOOTLOAD bit in the SYSCW register (section 9.1), using a normal SPI transaction as specified in section 8. Following that SPI transaction, the nSS line must remain high for at least a time TnRST2nSS illustrated in Figure 34 and specified in Table 31.

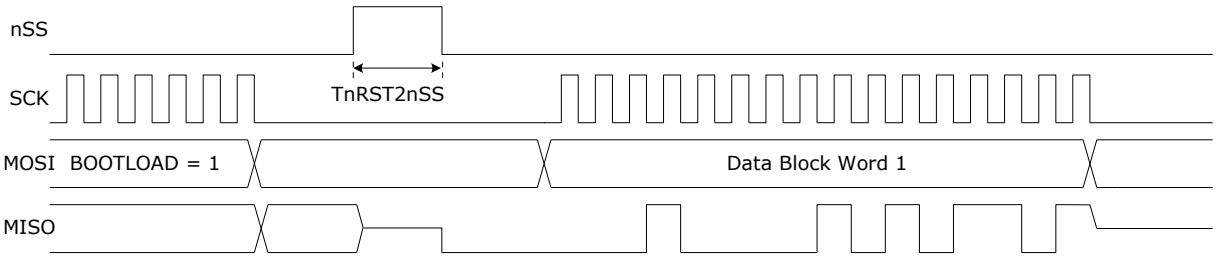

Figure 34 timing of first Data Block Word SPI transaction after setting BOOTLOAD=1

If the CAM312 does not include Application Code, the host must use the "Reset Entry Method". This begins with the host resetting the CAM312. This must be done either by pulling nRST low or by removing power (VCTU=0V) then reapplying it. The CAM312 chip's nSS line must be pulled high during or after reset, and must be pulled low before the first SCK transition. The time between coming out of reset and the nSS low edge before the first SCK edge is denoted TnRST2nSS. The minimum value of TnRST2nSS is specified in Table 31.

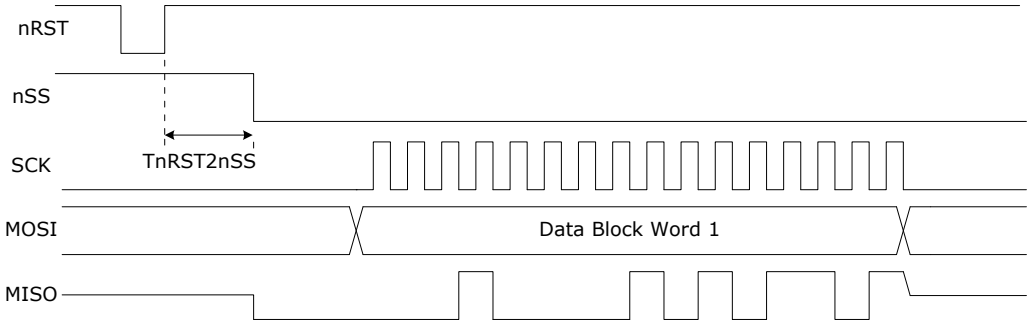

Figure 35 timing of first Data Block Word SPI transaction after reset

The host must now perform the Data Block Transfer Process, as detailed in section 12.5. There are three possible results: "successful", "CTU chip not in Bootloader Mode" or "Unexpected CTU Response".

If successful, the host may send the word 0xB002 to the CAM312 over SPI to request a reset. It must then wait for internal validity checks to complete, like after any reset (section 10.1). Once complete, the CAM312 chip is ready for normal operation running the new Application Code.

If the CAM312 chip returns the value of the SYSID register as the first word of the Data Block Transfer Process (factory default 0xABCD) then it is still running old Application Code, and is not in Bootloader Mode. The upload may either be aborted or begun again.

If the CAM312 chip returns an unexpected response over SPI during the Data Block Transfer Process (typically 0x0BAD) then the Bootloader process has failed and must be restarted. Sending 0xB002 to the CAM312 over SPI may initiate a reset. Once validity checks have been completed (section 10.1) the CAM312 will return the value of the SYSID register if the host sends 0x0000 over SPI, but only if the CAM312 chip still includes old Application Code. If not, the CAM312 chip does not include valid Application Code any more, and the Bootloader Process must be repeated.

When implementing the Bootloader process, it is essential to implement both the BOOTLOAD Bit Entry Method and the Reset Entry Method. The Reset Entry Method can not be used when starting with valid Application Code, so the BOOTLOAD Bit Entry Method must always be implemented. However there is always a risk of an unexpected behavior of the host system, for example another device sharing the same SPI device unexpectedly accessing the SPI bus during Bootloader data transfer. This may corrupt CAM312 Application Code, leaving the part with no valid Application Code. The Reset Entry Method always allows new Application Code to be programmed in this situation.

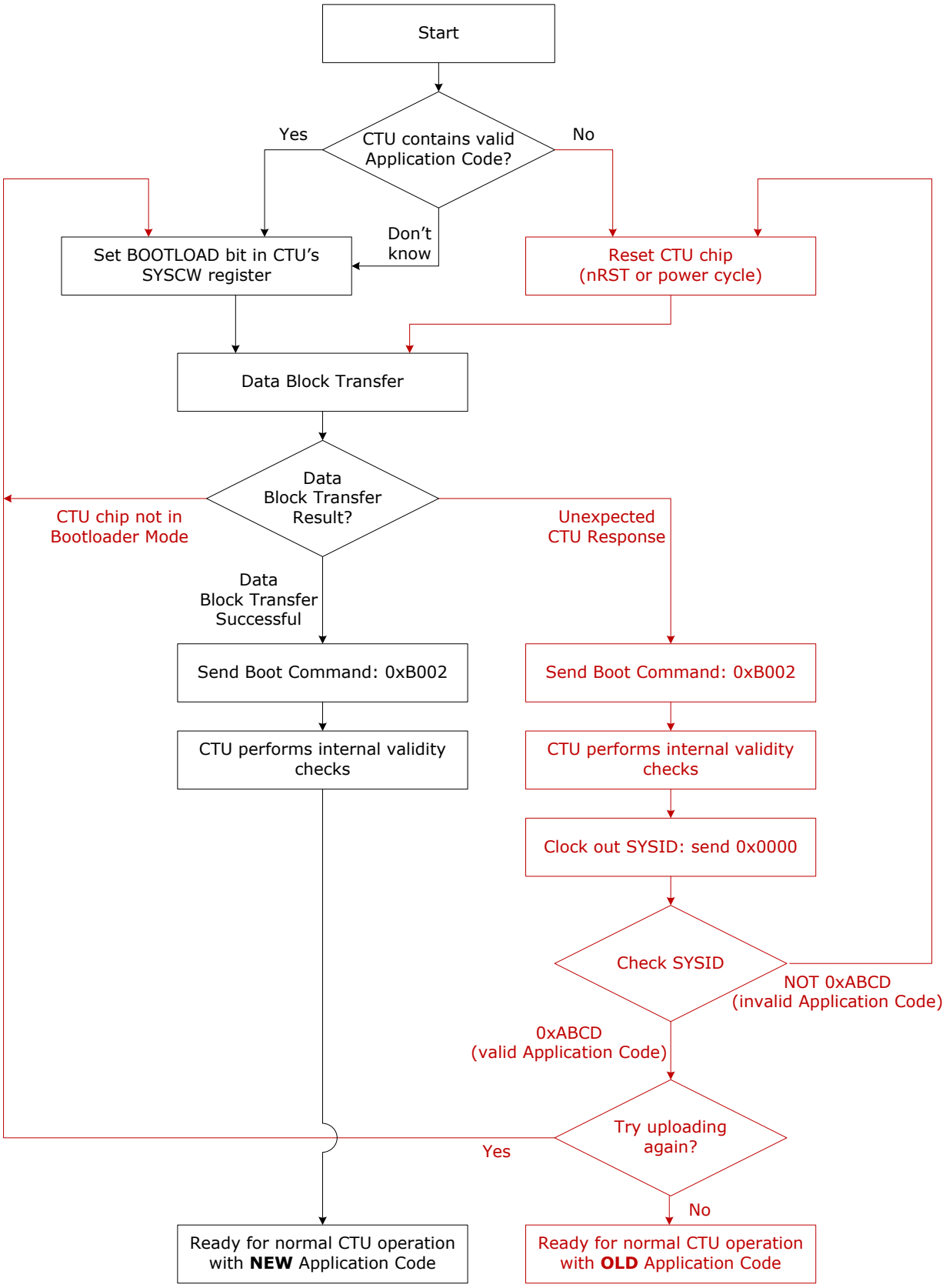

Figure 36 Bootloader flowchart

12.5 Data Block Transfer Process

The Data Block Transfer process is for sending new Application Code to the CTU, and is illustrated in Figure 37. It forms part of the Bootloader Process described in section 12.4.

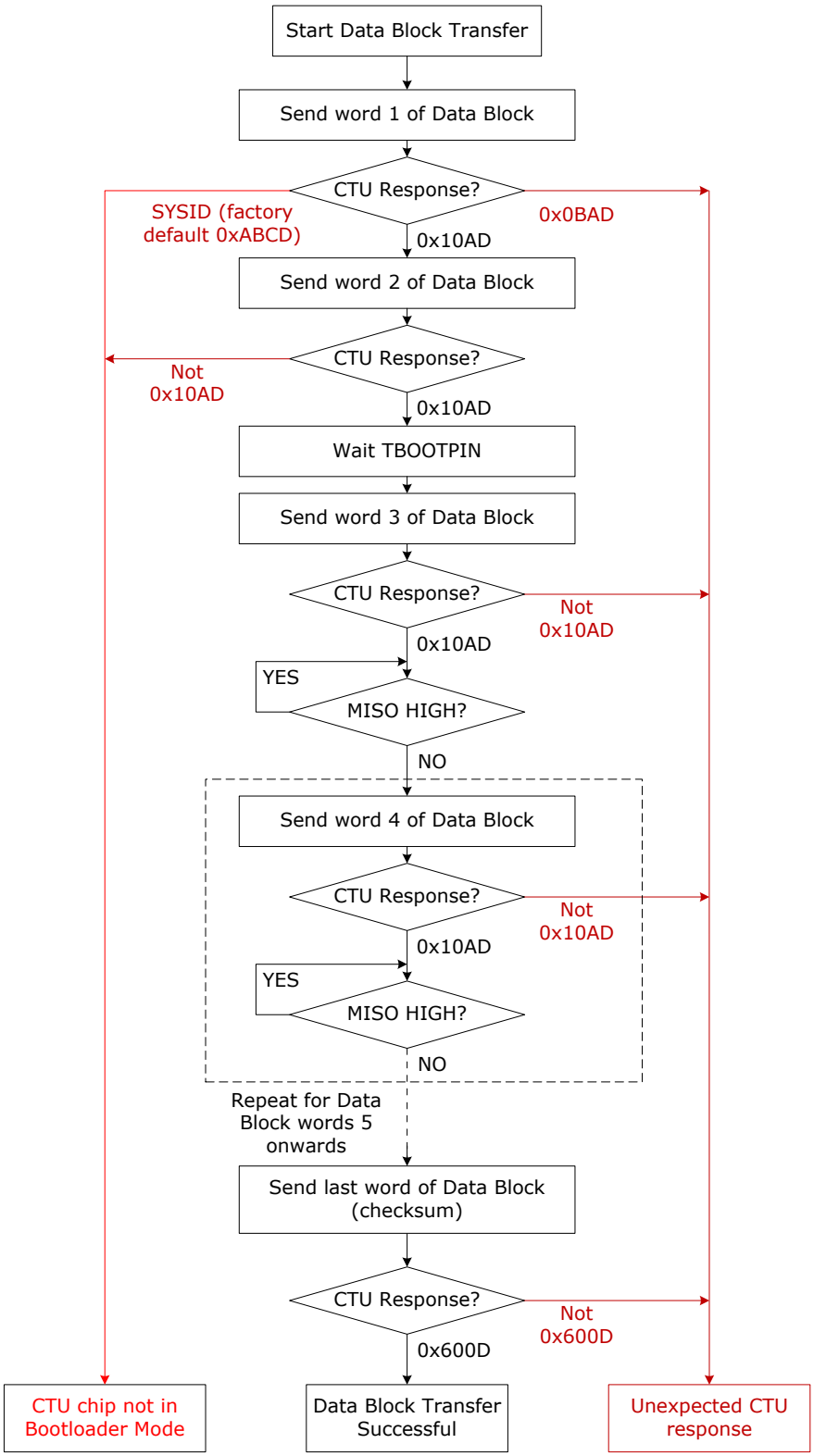

Figure 37 Data Block Transfer Process

Data is transferred in 16-bit words over the SPI interface, as described in section 12.6.

Each time the host sends a word, the CTU should respond with 0x10AD. If the response equals the value of Application Code's SYSID value (factory default 0xABCD) then the CAM312 chip is not in Bootloader mode. If it is anything else (typically 0x0BAD) then Data Block Transfer has failed.

The host must send the first two words of the Data Block and then pause before the third. The length of the pause is measured from the last SCK edge of the second word and the first SCK edge of the third word, and is denoted TBOOTWAIT. A minimum value of TBOOTPIN is required, and it is specified in Table 31. This pause is for Bootloader initialisation.

The remainder of the Data Block is then sent to the CAM312 chip, one word at a time. The host must check the state of the MISO line after each word. If it is high, the host must not send the next word until MISO has gone low. The time taken for MISO to go low is denoted TBOOTWAIT. Its maximum value is specified in Table 31.

The CAM312 chip's response to the last word of the Data Block will be 0x600D if successful.

12.6 SPI Communication with the CTU in Bootloader Mode

Communication with the CTU in Bootloader Mode uses the same SPI mode and bit ordering as described in section 8. The minimum clock low and high times and the clock period (TSCKL, TSCKH, TSCK) are also the same.

The CAM312 chip's SPI select line nSS must be low while data is being clocked into the CAM312 chip. nSS may remain low for the entire Bootloader process. Alternatively, nSS may be pulled high after any Data Block Word, providing it is pulled low again before the next.

As noted in section 12.5, the host must check the state of the MISO line after sending each Data Block Word. The next word may only be sent once MISO has returned to a low state. The time between the last SCK high going edge of a Data Block Word and MISO going low is denoted TBOOTWAIT. The maximum value is specified in Table 31.

Note that the CAM312 chip only pulls MISO low to indicate it is ready for the next Data Block Word if the nSS line is low. If nSS is high, MISO will be high impedance, to allow other slave devices to share the same SPI bus. If the host chooses to pull nSS high after a Data Block Word, it may test the state of MISO by pulling nSS low again. Providing SCK remains low throughout, this test may be repeated until the host detects MISO is low and the CAM312 is ready for the next Data Block Word.

There is one additional timing constraint: the host must ensure the time between each Data Block word is greater than the value TWW_BOOT(min) specified in Table 31. This can either be implemented with a pause between words as illustrated in Figure 38, or by operating with an SPI clock period TSCK of greater than TWW_BOOT divided by 16.

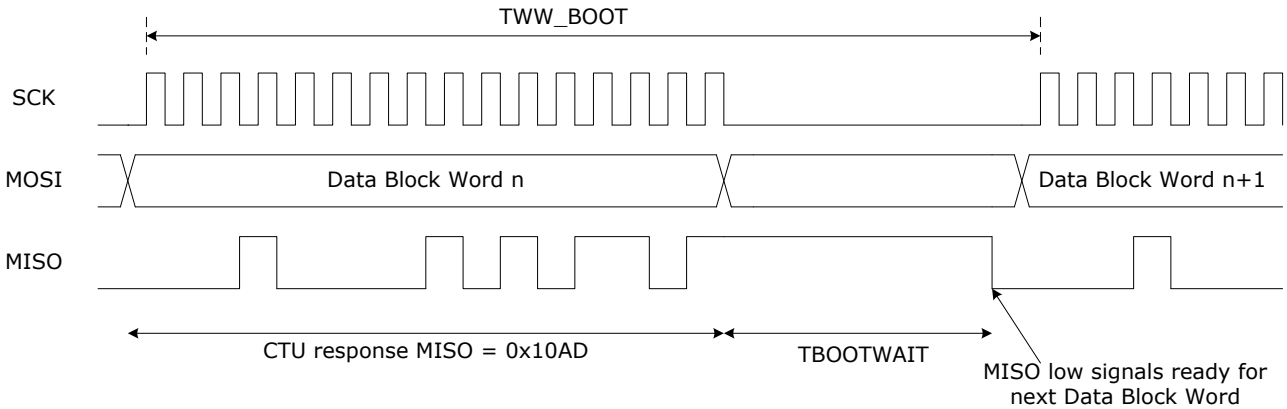

Figure 38 SPI communication, sending Data Block

12.7 Bootloader Timing Specifications

The specifications for the Bootloader timings referred to above are in Table 31.

Table 31 Bootloader timings

Parameter	Description	Min	Typ	Max	Units
TnRST2nSS	Delay between end of reset and first SCK high	3.2			ms
TBOOTPIN	Pause required between 2nd and 3rd Data Block words	500			µs
TWW_BOOT	Time between each Data Block Word and the next	4.8			µs
TBOOTWAIT	Variable pause required between Data Block Words			300	ms
TBOOTLOAD	Overall time to update Application Code	1.0			s

The following parameters are the same for Bootloader SPI as for normal operation, and are specified separately in Table 17: TSCKL, TSCKH, TSCK, TSCKR, TSCKF, TMISOR, TMISOF, TMOSIV2SCKH, TSCKH2MOSIX, TnSSL2MISOV, TSCKL2MISOV, TnSSL2SCKH, TSCKL2nSSH, TnSSH2MISOZ.

The total time taken to undertake the complete Bootloader process is denoted TBOOTLOAD. Table 31 specifies a minimum value, based on a host responding to MISO low immediately and operating with the minimum TWW_BOOT value.

13 Package Details

13.1 CAM312ME

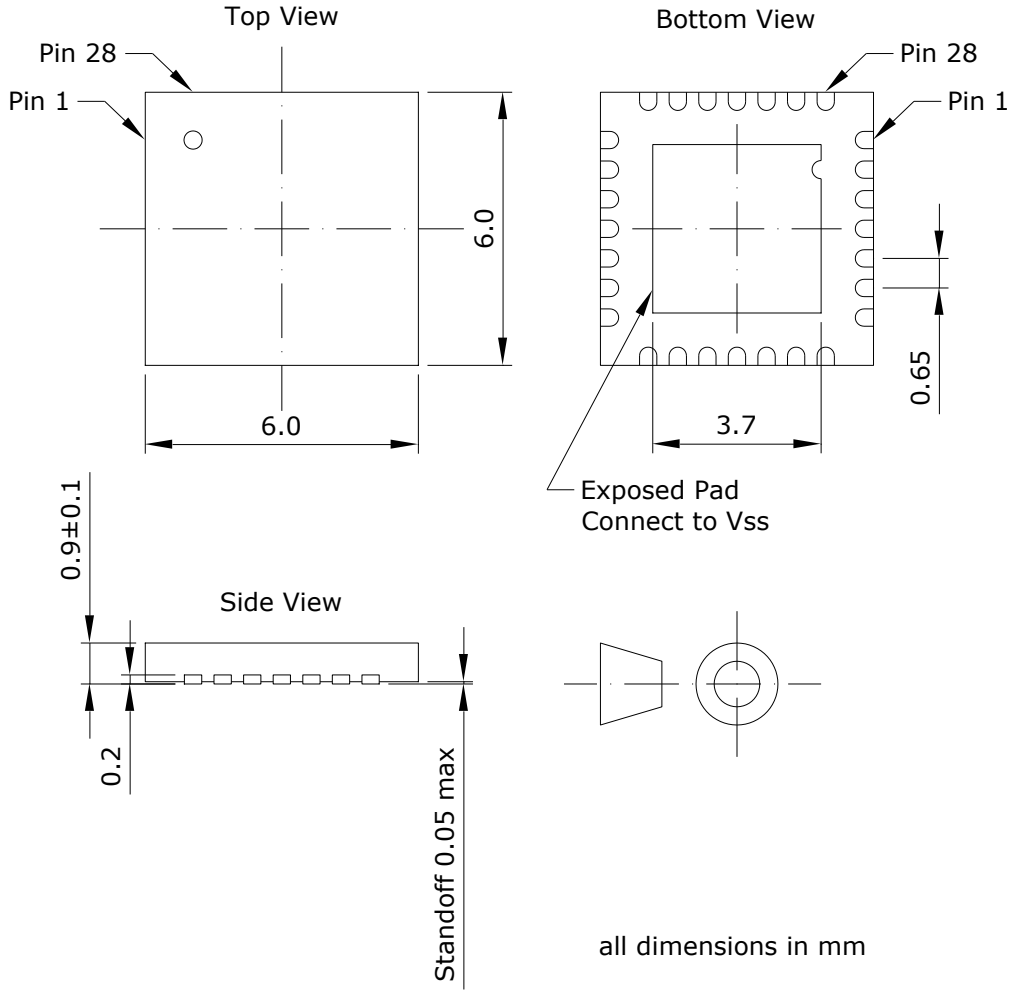

Figure 39 CAM312ME plastic quad-flat no-lead 28-pin (QFN: M suffix)

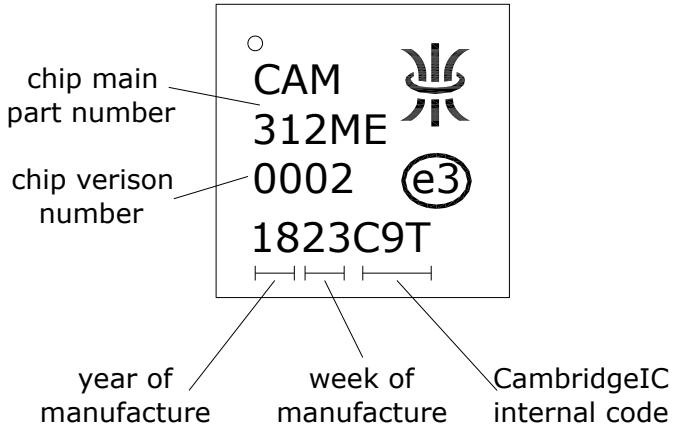

Figure 40 CAM204MI product markings

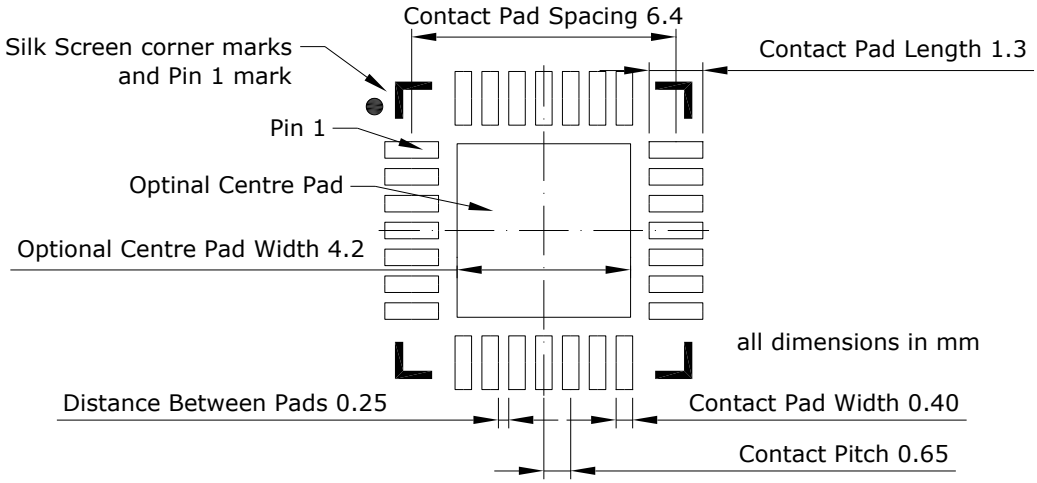

Figure 41 CAM312ME Recommended PCB Footprint

14 Tape and Reel Specifications

14.1 CAM312ME

CAM312ME chips are available in tape and reel on complete reels of 1600 parts. The carrier tape is illustrated in Figure 42, and dimensions are specified in Table 32.

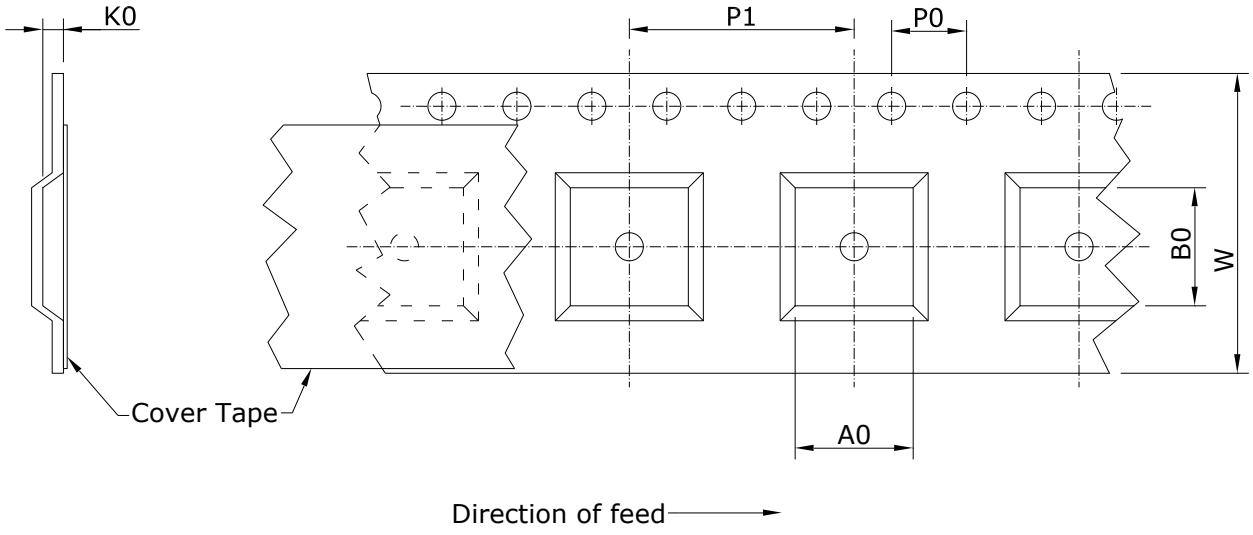

Figure 42 CAM312ME carrier tape dimensions

Table 32

Tape and Reel Specifications		Dimensions in mm						
Package	**Units per reel**	**Reel diameter**	**W**	**P0**	**P1**	**A0**	**B0**	**K0**
28-pin QFN	1600	330	16	4	12	6.3	6.3	1.1

15 Reflow Soldering Recommendations

The CAM312 is available in lead free packaging only. The recommended reflow soldering temperature profile is illustrated in Figure 43. Values are shown in Table 33.

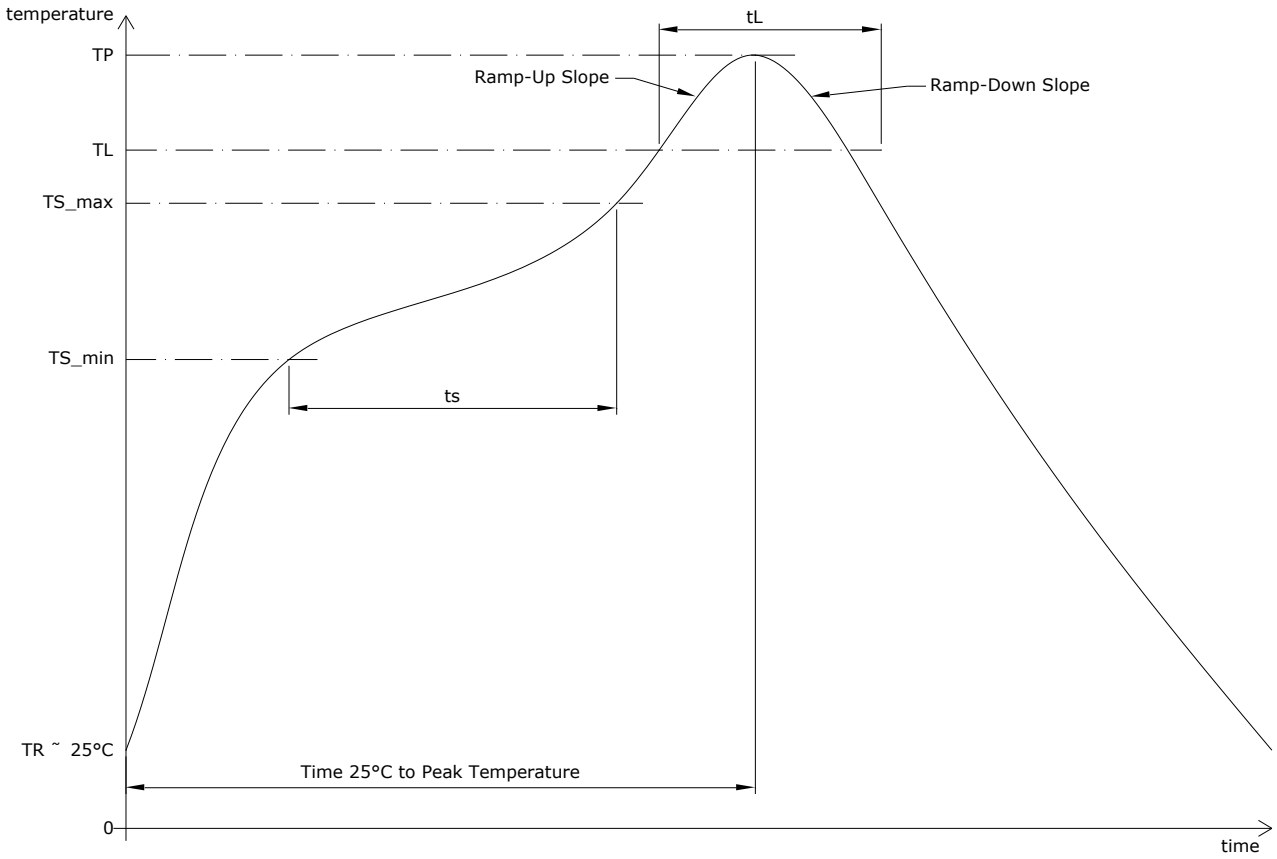

Figure 43 reflow soldering temperature profile definitions

Table 33

Profile feature	**Value**		**Comments**
TS_min	150°C		Preheat temperature range
TS_max	200°C		
ts	60s min	120s max	Preheat time
TL	217°C		Liquidous temperature
TP	225°C min	260°C max	Peak temperature
tL	60s min	150s max	Time maintained above Liquidous temperature
Ramp-Up Slope	3°C/s max		
Ramp-Down Slope	6°C/s max		

16 Environmental

Table 34

Item	Min	Max
Storage temperature	-65°C	160°C

17 RoHS Compliance

The CAM312 uses Matte Tim (Sn) pin finish. CambridgeIC certifies, to the best of its knowledge and understanding, that the CAM204 chip is in compliance with EU RoHS directive 2011/65/EU and 2015/863.

18 Document History

Table 35 main changes

Rev	Date	Comments
0001	14 Feb 2018	First draft including pinout, schematics, components, layout, mechanical and PCB details
0002	9 May 2018	Added "connections next to ground plane" option to layout recommendations. Added centre vias to recommended capacitor locations and wiring.
0003	12 Nov 2018	Added SPI Hardware section including SPI timing specifications and checksum Added System Operation and Bootloader sections Added Type 2 schematics and Type 2 and 6 component values Updated schematics so that C_MCOS and C_MSIN connect to 0V instead of VREF. This makes no significant difference to performance or function, and was done to simplify the CAM312 Development Board's design.
0004	4 Feb 2019	Added bootloader section

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20 Legal